Total dose radiation hardness of diamond-based silicon-on-insulator structures

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(Received 18 December 1989; accepted for publication 9 April 1990)

Total dose radiation hardness measurements were performed on silicon-on-insulator (SOI) test structures where the insulator is chemical vapor deposited (CVD) diamond. These measurements represent a first look at the fundamental radiation response of low-pressure CVD synthetic diamond materials for SOI applications. Silicon/diamond metal-insulator-semiconductor (MIS) capacitors were subjected to both cobalt-60 and 10 keV x-ray irradiation up to doses of 1×10^7 rad (SiO_2) while under positive, negative, and zero bias conditions. The diamond insulators used in these devices were found to be free from extensive hole or electron trapping. This behavior is consistent with the high electron and hole mobility of the polycrystalline diamond insulator.

Silicon-on-insulator (SOI) substrates for use in complimentary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) can allow for enhanced performance and wider operating conditions than bulk silicon substrates.[1] The device topology that is achieved, namely isolated islands of silicon, gives complete immunity from latch-up and increased immunity from transient and single event upsets. One of the most important applications of SOI ICs is in high radiation flux environments where an important figure of merit is the sensitivity of the technology to total dose ionizing radiation. The total dose radiation tolerance of a particular SOI technology is not a set quantity but arises due to the specific processes and materials employed and can be inferior to bulk silicon circuitry.[2]

Silicon on diamond (SOD) is a developing SOI technology that uses chemical vapor deposited (CVD) polycrystalline diamond as the insulating layer.[3] In this approach polycrystalline diamond is mated with a single-crystal Si active layer. Figure 1 is a cross-section scanning electron micrograph of a SOD wafer. The main advantages of SOD technology are that diamond has high electron and hole mobility and excellent thermal transport properties when compared with the insulating layer of other SOI technologies,[4] such as silicon dioxide and sapphire. This approach permits flexibility in optimizing the properties of the SOI wafers, which is especially important in constructing a high quality insulator/semiconductor interface. The technique used to construct these wafers has been fully detailed elsewhere.[3] In order to optimize the interface properties of the structure investigated here, a thin 7.0 nm thermal silicon dioxide (SiO_2) film was grown on the single-crystal silicon layer before polycrystalline diamond deposition, sharply reducing the preirradiation silicon fast interface trap density. Without the thin SiO_2 layer, the silicon-insulator interface potential is pinned in the midgap region by an extremely large, fast interface trap density.[3] The resistivity of the combined dielectric layer is not affected significantly by the oxide layer. The dielectric structure of the metal-insulator-semiconductor (MIS) test capacitors used in this study is very similar to a metal-nitride-oxide semiconductor (MNOS) nonvolatile memory element except for the important distinction that the SiO_2 diamond interface is largely trap free.[5]

Electronic applications of diamond have focused on the superior transport properties of semiconducting diamond.[3] Recent advances in the CVD fabrication of diamond films have shown that insulating films can be produced if proper techniques are used to exclude shallow dopants from the process.[6,7] As with GaAs, the routine growth of diamond insulating materials which can be either an insulator or semiconductor is far from trivial. The added difficulty can be justified in radiation tolerant SOI where efficient transport of radiation-produced carriers is

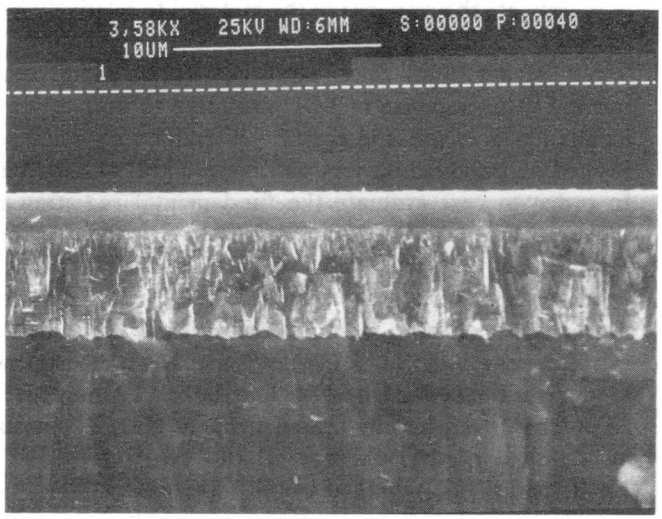

FIG. 1. Cross-sectional scanning electron micrograph of a silicon on diamond wafer. The top layer is single-crystal silicon, the middle layer is polycrystalline diamond, the thick bottom substrate layer is polycrystalline silicon. The white scale marker bar represents 10 μm.

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desired simultaneously with good insulating and thermal properties.[8] During irradiation large numbers of electron-hole pairs are created in the insulator. If all of the charge is conducted away without significant trapping, then the cumulative effect of the irradiation will be small. In silicon dioxide insulators the small effective hole mobility of 2×10^{-5} cm^2 (V s)$^{-1}$ strongly enhances the probability of permanently trapping radiation-produced holes over electrons, which have a mobility[9,10] of 20 cm^2 (V s)$^{-1}$. In single-crystal diamond, due to the excellent electron and hole mobility[11] of about 1500 cm^2 (V s)$^{-1}$, one might expect that the majority of the radiation-produced carriers may be conducted out of the device with little electron or hole trapping. The reduced mobility expected in polycrystalline diamond should still be sufficiently high to prevent excessive carrier trapping, as confirmed below.

In this letter, we report on total dose radiation tolerance of SOI structures using diamond insulators grown so as to optimize diamond's good transport properties.[6,7] Metal insulator semiconductor (MIS) test devices were fabricated from wafers with a diamond/p-type silicon (1×10^{16} boron cm^{-3})/p^+ silicon (1×10^{19} boron cm^{-3}) structure. The diamond films are grown using dc plasma techniques utilizing precursor mixtures of methane and hydrogen gas. As previously discussed, the diamond films are not grown directly on the silicon substrate but utilize a thin 7.0 nm thermal oxide layer between the diamond and active silicon layer. The diamond film used as the insulating layer in this study was 0.4 μm in thickness. To evaluate the radiation hardness of the diamond layer in SOI applications, MIS capacitor test structures were made by sputtering aluminum dots on the diamond and an aluminum film on the silicon substrate. Individual devices were bonded and packaged for radiation testing.

Cobalt-60 irradiations were performed in an AECL Gammacell 220 at a dose rate of 1.0 Mrad SiO_2/h. The 10 keV x-ray irradiations were performed with an ARACOR Model 4100 semiconductor x-ray irradiator at a dose rate of 12 Mrad SiO_2/h. The Co-60 irradiations were performed to investigate the response of the material to relatively high energy ($\sim$1 MeV) photons, and the x-ray irradiations allowed higher total dose exposures to be made more quickly. The response of SOI insulators to both types of irradiation is of great interest.[2] All irradiations were performed on unlidded devices which were held at fixed bias. In order to best evaluate the fundamental radiation response of the structure and to predict eventual circuit performance, devices were irradiated at 5, 0, and -5 V. The irradiations were interrupted periodically and the devices were characterized to monitor device degradation. 1 MHz capacitance-voltage (C-V) measurements were performed to monitor the device threshold and flatband voltage shifts. In order to evaluate any time-dependent bias temperature instabilities, all devices, after irradiation, were baked at 150 °C with $+5$ V applied bias for five weeks.[2,12]

Plotted in Fig. 2 are the measured results for flatband voltage shift versus time for 10 keV x-ray irradiation and in Fig. 3 the results for Co-60 irradiations. Charge generation and electron-hole recombination differences between the

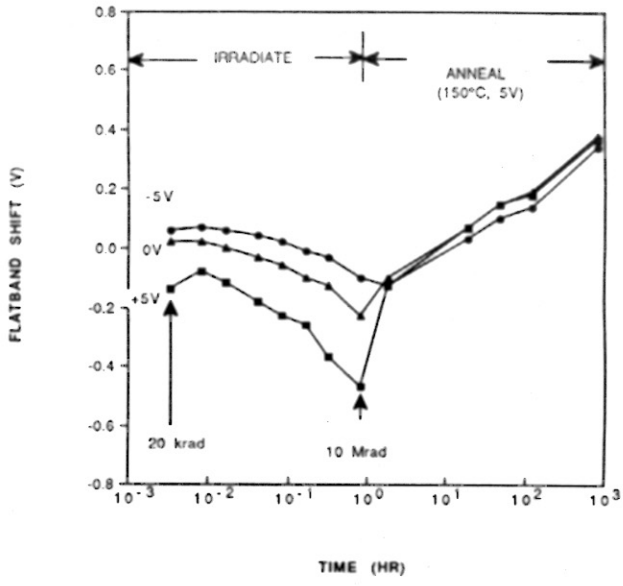

FIG. 2. Flatband voltage shift as a function of irradiation and anneal time for applied device bias voltages of $+5$, 0, and -5 V. The devices were exposed to 10 keV x rays at a dose rate of 200 krad per min and then annealed at 150 °C while maintaining a $+5$ V bias. The maximum irradiated dose was 1×10^7 rad SiO_2. Interface traps (N_{IT}) are not observed and the flatband shifts are due only to trapped positive and negative charge.

two radiation sources, due to the differences in radiation energy,[2,13] are most likely responsible for the nearly equivalent response due to 1×10^7 rad SiO_2 x ray and 2×10^6 rad SiO_2 Co-60 irradiations. During the initial time period shown in Figs. 2 and 3, the devices were irradiated at the

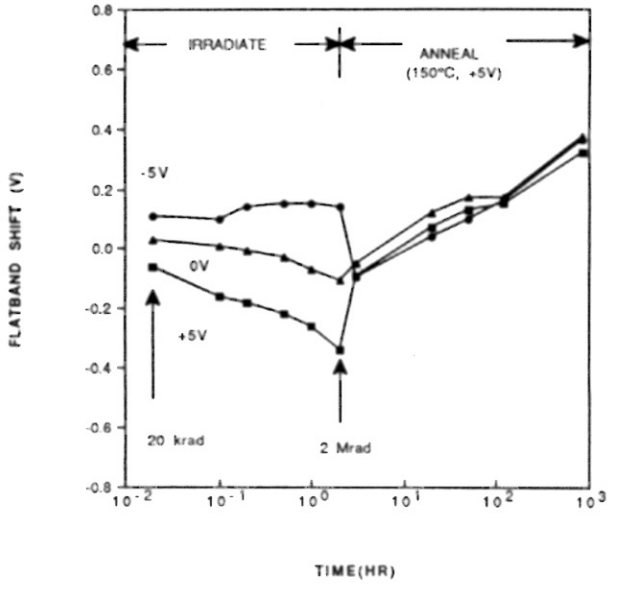

FIG. 3. Flatband voltage shift as a function of irradiation and anneal time for applied device bias voltages of $+5$, 0, and -5 V. The devices were exposed to radiation from a Co-60 source at a dose rate of 1 Mrad per h and then annealed at 150 °C while maintaining a $+5$ V bias. The maximum irradiated dose was 2×10^6 rad. Interface traps (N_{IT}) are not observed and the flatband shifts are due only to trapped positive and negative charge.

indicated dose rate, and during the later time period the devices were annealed.

Overall the most striking feature of the data is the extremely small measured flatband voltage shifts when compared to typical shifts of > 10 V for SiO_2 insulators of equivalent thickness at positive or zero bias.[2,12] The small observed shift of ~ 0.5 V suggests that the radiation tolerance of silicon on diamond structures may be greater than 1×10^8 rad SiO_2. Threshold voltage shifts did not differ from the flatband voltage shift to within the experimental voltage accuracy of ± 30 mV. This indicates that the insulator trapped charge is the dominant defect produced by irradiation.[14] During the elevated temperature post-irradiation anneal, the radiation-induced insulator trapped charge is quickly removed,[12] as evidenced by the independence of the annealing response in Figs. 2 and 3 from the radiation damage. We attribute the small ($+0.3$–0.4 V) flatband shifts during the positive biased 150 °C anneal to electron injection into the insulator from the substrate.

The overall radiation tolerance of the SOD test structure has been demonstrated here to easily exceed 1×10^7 rad SiO_2. We conclude that SOD is a promising candidate for a radiation-hardened SOI technology.

We thank N. Moore and L. C. Riewe for technical assistance and N. A. Godshall, P. S. Winokur, and S. S. Tsao for stimulating discussions. This work is partially supported by SDIO/IST through the Office of Naval Research and the U. S. Department of Energy through contract DE-AC04-76DP00789.

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