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SILICON ON INSULATOR TECHNOLOGY USING CVD DIAMOND FILMS

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The fabrication and features of a unique silicon on insulator (SOI) structure composed of a thin single crystal silicon film on a thin insulator made of plasma synthesized diamond are discussed. The excellent electrical resistivity and unsurpassed thermal conductivity of diamond offers the opportunity for extending the performance capabilities of silicon integrated circuits.The key characteristics of such a structure that are discussed are the resistivity of the insulator and the properties of the silicon-diamond interface. Such structures permit the fabrication of high performance semiconductor circuits characterized by high speed, low dynamic power consumption, greater packing density, increased power dissipation and immunity from latch up and radiation induced failure.

Introduction

Two of the most important properties of diamond from the perspective of its utility in electronic applications are the high electrical resistivity of undoped diamond and its high thermal conductivity. These properties, if realized in CVD synthesized polycrystalline diamond films, can find use in a unique application in silicon on insulator structures which should permit the extension of the operational capabilities of a large class of silicon devices and circuits. Indeed diamond films may find the most immediate utility in semiconductor technology as passive components of structures in combination with other semiconductors such as silicon or gallium arsenide.

Silicon on insulator (SOI) technology has been in continuous development for many years. In this approach the objective is to create thin (< 1 micrometer) high quality films of silicon on insulating substrates. The drive towards developing such structures is based on a number of advantages they confer in the fabrication and operation of integrated circuits. In brief and incomplete form these advantages are discussed below with reference to MOS, bipolar and three dimensional integrated circuit technologies.

There are several advantages to the use of SOI technology in the fabrication of MOS and, in particular, CMOS structures. These include the fabrication of circuits that exhibit higher speed, lower dynamic power consumption, greater packing density, increased radiation tolerance and a simpler fabrication sequence as compared to bulk single crystal technology. A reduction in the complexity of processing can be achieved in SOI since it is possible to dispense with conventional device isolation techniques such as back to back pn junctions as in the iso planar process, the use of doped channel stops and the use of thick

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dielectrics as in the LOCOS process. In the case of SOI wafers complete isolation of the devices can be achieved by the etching of individual islands or mesas in the silicon or by the complete oxidation of the silicon between the silicon islands with the subsequent fabrication of transistors and other active components in the islands. It has further been shown that the number of fabrication steps can be reduced by a factor of over fifty percent by utilizing SOI wafers as compared to bulk crystal technologies (1).

The use of SOI enables an increase in the operating speed of MOS structures because of the reduction in the output node capacitance that the presence of the insulating substrate affords. This is due to the ability of achieving much reduced effective volumes of pn junctions in SOI structures as compared to bulk structures and the fact that the bottom and three sides of junctions can be bounded by dielectric layers. The reduced output node capacitance of SOI structures also translates into reduced dynamic power consumption.

SOI technologies to date have not been widely applied to bipolar and analog structures because of the relatively poor quality of the silicon in current generation SOI wafers. However, there are several advantages to the use of SOI in bipolar circuits. Simpler fabrication sequence and much higher packing densities are some of the immediate benefits as in the case of MOS circuits. The ability to dispense with the use of isolation diffusions and the potential for using dielectric isolation are strong motivators in applying SOI technologies to bipolar circuits. High switching speeds can be achieved in bipolar circuits by using SOI techniques since the insulating substrate permits a very rapid rate of recombination of carriers in the collector due to reduced collector volume of transistors built in the overlying silicon. Conventional approaches utilize heavily doped buried layers or subcollectors to decrease resistance beneath the collector.

An important benefit that SOI structures offer is in being able to combine MOS and bipolar devices on the same chip. BiCMOS technology would benefit greatly from the ability that SOI offers of fabricating dielectrically isolated silicon islands in which MOS and bipolar devices can be fabricated. High voltage operation, high operating speed and low dynamic power dissipation are the potential advantages of SOI in both MOS and bipolar circuits. SOI structures also provide the important benefits of minimizing or eliminating electrical malfunctions such as latch up in CMOS circuits and functional upsets due to ionizing radiation. The charge generated by ionizing radiation is related to the volume of the silicon affected and SOI offers significant improvement over bulk silicon since the volume of the silicon exposed to ionizing radiation is very small as compared to bulk silicon technology.

There is increasing interest in three dimensional or vertically integrated circuits wherein transistors are stacked on top of each other and separated by appropriate insulators. The drive towards three dimensional integration is based on a number of factors including the ability to realize higher packing density and complexity and the possibility of achieving parallel processing. SOI structures should figure prominently in three dimensional integration.

SOI Structures using Polycrystalline Diamond Films

One of the most attractive applications of diamond films is their use as insulators beneath thin single crystal silicon films in silicon on insulator structures. In order to form single crystal silicon films on insulators the normal approach has been one of heteroepitaxy

of silicon on an appropriate insulating single crystal substrate such as sapphire. In order to achieve SOI structures incorporating diamond films as insulators the traditional approach would require that single crystal diamond films be grown followed by the heteroepitaxial growth of silicon films on the diamond films. To date single crystal diamond film growth has not been demonstrated. In addition the very large lattice mismatch between silicon and diamond (65%) would preclude heteroepitaxial growth of silicon on diamond. Consequently in order to advantageously use the excellent electrical insulating and thermal conductivity characteristics of diamond films, approaches for the use of polycrystalline diamond films in conjunction with single crystal silicon films have to be developed. In this paper we present the concepts for such a process and discuss some preliminary data on the features and characteristics of such a structure.

The process sequence for the fabrication of silicon on insulator wafers using polycrystalline diamond films is as follows. The process is schematically illustrated in Figure 1.

- A high quality single crystal silicon wafer is subjected to a high concentration boron diffusion or implantation.
- A high quality defect free epitaxial layer is grown on the boron implanted wafer.
- A polycrystalline diamond film (approximately 1 to 2 micrometer in thickness) is grown on the epitaxial layer by plasma enhanced CVD techniques.
- A thick polysilicon layer is deposited on the diamond by CVD techniques
- The substrate silicon is removed by etching using KOH or EDP etches. The boron etch stop limits the etching to the silicon substrate without attacking the epitaxial layer.
- The boron diffused (implanted) layer is subsequently removed by high selectivity etches.

The key advantages of this approach include the following:

- A high quality silicon layer can be created since the epitaxial film is deposited on silicon crystals rather than heteroepitaxily on materials like sapphire or formed on insulators such as silicon dioxide.

- The quality of the silicon layer is only limited by the quality achievable in homoepitaxy of silicon on silicon. This technology is very mature and high quality epitaxy is routinely achieved.

- Diamond films are excellent insulators with natural diamond exhibiting a resistivity of 10^{16} ohm cm. Based on the measurement of thermal conductivity of plasma synthesized diamond films if has been demonstrated that these films have a thermal conductivity nearly equal to that of natural diamond single crystals (2,3). By analogy it is expected that the resistivity of these films is also close to that of natural diamond. Further discussion of the resistivity of diamond films is presented below.

- One of the most important properties of diamond films that make them superior to all other insulators is their exceptionally high thermal

conductivity. Table 1 is a comparison of some of the critical properties of the two leading SOI technologies (SOS and SIMOX) and the expected characteristics of silicon on diamond structures. From this comparison it is evident that the vastly superior thermal conductivity of diamond will be an asset in heat dissipation from circuits built in the silicon layers over the diamond films. This property should be particularly important in combining high power bipolar structures with MOS structures on the same chip.

A similar technique was developed over a decade ago utilizing silicon dioxide insulators for the SOI structures (4). One of the most important advantages of diamond films in place of silicon dioxide as insulators is the very high thermal conductivity of diamond.

Table 1. A Comparison of Silicon-on-Insulator Technologies

	SILICON ON SAPPHIRE	SIMOX	SILICON ON DIAMOND
Dielectric Constant	4.5-8.4 (Sapphire)	3.9 (SiO_2)	5.5 (Diamond)
Thermal conductivity	0.3 (Sapphire)	0.014 (SiO_2)	20 W/ cm °K (Diamond)
Density of Interface States	$2*10^{12}$	$8*10^{10}$	Unknown (see below)
Electrical resistivity of the dielectric	10^{15}	10^{14}-10^{16}	10^{16} (ohm cm)
Silicon Thickness	> 0.3 microns	> 0.1 micron	<.05 microns ?
Thickness of insulator	15-20 mils	< 1 micron	<1 to >10 microns
Silicon Quality	Low mobility, high density of interface defects	Potential for impurity contamination; high oxygen content	Potential for high quality
Manufacturing Cost	High	Low (High capital cost)	Potentially Low

Wafer Fabrication

SOI wafers utilizing diamond films have been fabricated according to the above described process. The key aspects of the fabrication procedure are as follows:

100 mm diameter, p-type, 1-3 ohm cm, polished silicon wafers were subjected to boron implantation and silicon epitaxial growth using conventional approaches. Implant doses of 2E16 at a beam voltage of 160 KeV were used. Implant damage anneal and boron activation were achieved during the silicon epitaxial process. p type epitaxial layers of thicknesses of ~ 2 μM have been investigated to date. Polycrystalline diamond films 1 to 2 μM in thickness were deposited on the epitaxial wafers utilizing a DC plasma technique with mixtures of methane and hydrogen as the reactive gases. Figure 2 shows an example

of a diamond film on a 100 mm diameter silicon wafer with a plot of the uniformity of thickness distribution of the film across the wafer and Raman spectra as a function of position on the wafer. These data indicate that thin diamond films of high and uniformity quality can be deposited on large area silicon wafers.

Following diamond deposition a thick polysilicon layer was deposited on the diamond film at a temperature of 900°C. The polysilicon film thickness was ~ 20 mils. Figure 3 shows a cross sectional scanning electron micrograph of a region of a wafer that has been subjected to the processes discussed thus far.

Following polysilicon deposition the single crystal silicon substrate is removed by etching in EDP or KOH etches. These etches are both concentration and type dependant and the high concentration etch stop between the silicon substrate and the epitaxial layer functions in such a manner as to terminate etching leaving a structure composed of a thin single crystal silicon film (the epitaxial layer) on top of a thin polycrystalline diamond film backed up by the polycrystalline silicon layer which functions as the support member conferring rigidity to the structure. Figure 4 shows an SEM micrograph of the cross section of the completed structure. Prior to device fabrication the high concentration boron surface has to be removed by selective etching.

Characteristics of the SOI structure

The fundamental requirements of an SOI structure can be enumerated as follows:

- High quality thin silicon
- High quality insulator under the silicon layer
- Good interface properties
- Large area wafers (100 mm and greater in diameter)
- Defect free silicon films exhibiting high lifetime and mobility for bipolar applications
- Wafer flatness of the required degree for submicron lithography over large areas

In addition to the above general requirements for SOI structures high thermal conductivity diamond films have to be synthesized in order to take advantage of this property of diamond films in the proposed application. CVD diamond films have been grown with thermal conductivities ranging up to 14 W/cm°K (2,3). In the present work we will discuss issues relating to the characteristics of the insulator, diamond and the properties of the silicon diamond interface.

Resistivity of Diamond Films

There have not been many reports on the resistivity of diamond films. Work to date in this area is summarized in table 2. From this data it is evident that the reported resistivities range widely from about 10^5 ohm cm to 10^{13} ohm cm with most of the data in the literature tending towards low resistivity diamond films which have not been intentionally doped. For the use of diamond films in the application discussed in this paper it is necessary that high resistivity films be grown. The observed low resistivities can be a result of the presence of varying concentrations of non diamond bonded carbon sites in the films or a result of unintentional contamination.

Table 2. Reported resistivity data on CVD diamond films

Reference	Resistivity (300°K) Ohm-cm	Activation Energy eV
Sokolina et.al. (5)	10^{13} - 10^{14}	0.45 - 1.15
Gildenblat et.al. (6)	10^{3} - 10^{6}	0.29 - 0.41
Nakahata et. al. (7)	10^{6} - 1.0 (boron doped)	0.6 - 0.2

In this work we report on the fact that the resistivity of CVD dimond films is not governed, to a first order, by the presence of non diamond bonded phases in the films. We have shown, elsewhere, that current conduction in these films is strongly related to the presence of hydrogen in the films (8). Figure 5 shows three Raman spectra from three different diamond films one of which was synthesized by the use a microwave excited plasma and the other two were synthesized by the use of DC plasmas. All the spectra display strong Raman shifts at 1333 wavenumbers attributed to diamond bonding (sp^3 sites) in the films. In addition to the main Raman peak due to diamond bonding, the films synthesized by the use of a DC bias plasma display Raman peaks attributed to non diamond bonded material whereas the microwave synthesized sample shows the Raman shift only due to sp^3 bonding sites. The corresponding resistivities of these films are shown adjacent to the Raman spectra. There is no apparent relationship between the Raman spectrum and the resistivity of the as grown diamond film indicating that the presence of small amounts of non diamond bonded phases in the films have no apparent effect on current conduction in the diamond films.

The highly variable and the generally low resistivity of as synthesized diamond films can be attributed to the effects of hydrogen passivation of traps in these films. This has been shown to be the case by the observation that current conduction in diamond films is a strong function of the post synthesis thermal history of the films. Heat treating diamond films at temperatures as low as 100°C has been found to have a strong impact on current conduction and hence their resistivity (8). Heat treating diamond films at temperatures of ~350°C results in an increase in the resistivity by up to seven orders of magnitude. That hydrogen is primarily responsible for this effect was demonstrated by rehydrogenation of heat treated diamond films in a hydrogen plasma. Figure 6 shows I-V characteristics of a diamond film as a function of process history. The as grown film displays a resistivity of ~ 10^{6} ohm cm. Heat treating the film at 600°C for 30 minutes in flowing nitrogen causes a significant change in the I-V characteristics with an increase in the resistivity to about 10^{13} ohm cm attended by evidence of trap limited conduction characteristics. Rehydrogenating the film by subjecting it to a hydrogen plasma at 400 °C for 4 hours reverses the trend, with the I-V characteristics of the hydrogenated films being similar to that of the as grown films and attended by a marked reduction in the resistivity over that of the annealed film. The data shown in figure 6 is for a diamond film synthesized by the use of a DC bias plasma. In figure 7 are shown I-V curves of an annealed and hydrogenated diamond film synthesized by the use of microwave assisted plasmas. Current conduction in these films is also strongly governed by the presence of hydrogen suggesting that the effect of hydrogen in diamond films is a general phenomenon which is not affected by the methods utilized for diamond synthesis as long as atomic hydrogen is an ingredient of the plasma ambient during diamond synthesis.

The effects of atomic hydrogen in passivating interband states in various semiconductors has been well established. Defect states due to dangling bonds in amorphous silicon, grain boundaries in polycrystalline silicon and interband levels due to impurities have all been shown to be subject to hydrogen passivation (9-11). For example, gold in silicon has been shown to introduce both a donor and an acceptor level and when the concentration of gold is comparable to or greater than the shallow acceptor concentration a marked increase in the resistivity of the silicon is observed (12). Hydrogenation of the gold doped samples has been shown to reduce the resistivity as a result of passivation of gold related deep levels (13-14). In the case of the diamond films we postulate that the resistivity of the hydrogenated films is governed by shallow acceptor levels whereas removal of the hydrogen by annealing electrically activates deep donors, pinning the Fermi level and giving rise to the observed high resistivity.

These results indicate that for the growth of high resistivity diamond films post growth annealing is required in order to remove the effects of hydrogen passivation of deep traps in these films. The annealed films display trap limited behavior with the DC bias synthesized films displaying two steeply rising current steps seperated by a small, finite voltage. This suggests the presence of a trap behaving as a double donor. A likely candidate for the chemical specie that functions as a double donor is oxygen which has been identified to be a double donor in silicon. The films synthesized by the use of microwave excited plasmas display a continuous density of states in the gap as opposed to discrete levels. The typically higher growth rates of microwave plasma synthesised diamond films may lead to more inhomogeneous films with a wider distribution of defect states in the band gap whereas the slower growth rates of DC plasma synthesized films can lead to structures that are less random, with discrete energy levels in the gap.

Properties of the Diamond - Silicon Interface

Another important parameter of SOI structures in the property of the silicon - insulator interface. A high density of interface states is undesirable. The properties of the diamond- silicon interface have been characterized by making capacitance - voltage measurements. Figure 8 is a C-V plot of a diamond- silicon structure whereby the diamond film was grown directly on a polished silicon wafer. No modulation of the capacitance is observed as a function of voltage as a result of a large density of interface states. One approach to overcoming this problem is to interpose a thin layer of SiO_2 between the silicon and the diamond film. This was achieved by growing an 80Å thick layer of thermal oxide on the silicon wafer followed by the growth of a diamond film on the thermal oxide. The C-V plots, obtained at 100 KHz and 100 Hz are shown in figure 9. The C-V behavior is as expected for an oxide -silicon structure and the presence of diamond on the oxide does not appear to have any effect on the properties of the interface. From this data the interface state density has been computed as a function of position in the band gap as shown in figure 10. An interface state density of $\sim 5 * 10^{11}$ cm^{-2} eV^{-1} has been estimated from these measurements.

The incorporation of a thin SiO_2 layer between the diamond and the silicon has been shown to overcome the problems associated with a high interface state densities between diamond and silicon while maintaining the other advantages of the silicon on diamond structure.

Conclusions

The fabrication process and some of the properties of a novel SOI structure utilizing PECVD diamond films as insulators have been discussed. It has been shown that thin single crystal silicon films on thin polycrystalline diamond films backed up by thick polysilicon layers can be fabricated to furnish silicon on insulator wafers that can benefit from the expected superior quality of the silicon and the exceptional thermal conductivity of the diamond films. Diamond films embedded between epitaxial silicon and polysilicon do not appear to introduce excessive stresses in the structures and planar, stress free layers have been fabricated. It has been shown that high resistivity diamond films can be produced by appropriately heat treating the diamond films to expel dissolved hydrogen from the films. The properties of the diamond-silicon interface can be enhanced by the interposition of very thin layers of silicon dioxide between the diamond and the silicon. The electrical properties of the silicon layers on the diamond films have not been investigated to date and will be the subject of subsequent publications.

High quality silicon layers of thicknesses less than 50 nanometers on insulators would have far reaching implications in the fabrication of integrated circuits. In particular, problems of leakage currents, latch up in CMOS devices and upsets due to ionizing radiation would be all but eliminated. Current generation SOI technologies cannot be utilized for the fabrication of such thin films of silicon since the regions of the silicon close to the silicon-insulator interface (< 0.3 micrometers) are typically of poor quality with low lifetimes and mobilities (15). Consequently these regions are not suitable for the fabrication of devices. The silicon on diamond approach, on the other hand offers the opportunity of fabricating very thin silicon structures since the process does not involve heteroepitaxy and diamond deposition temperatures can be maintained to be fairly low (~ 600°C) resulting in high electronic quality silicon with prospects for the creation of structures with very thin silicon layers.

Acknowledgment

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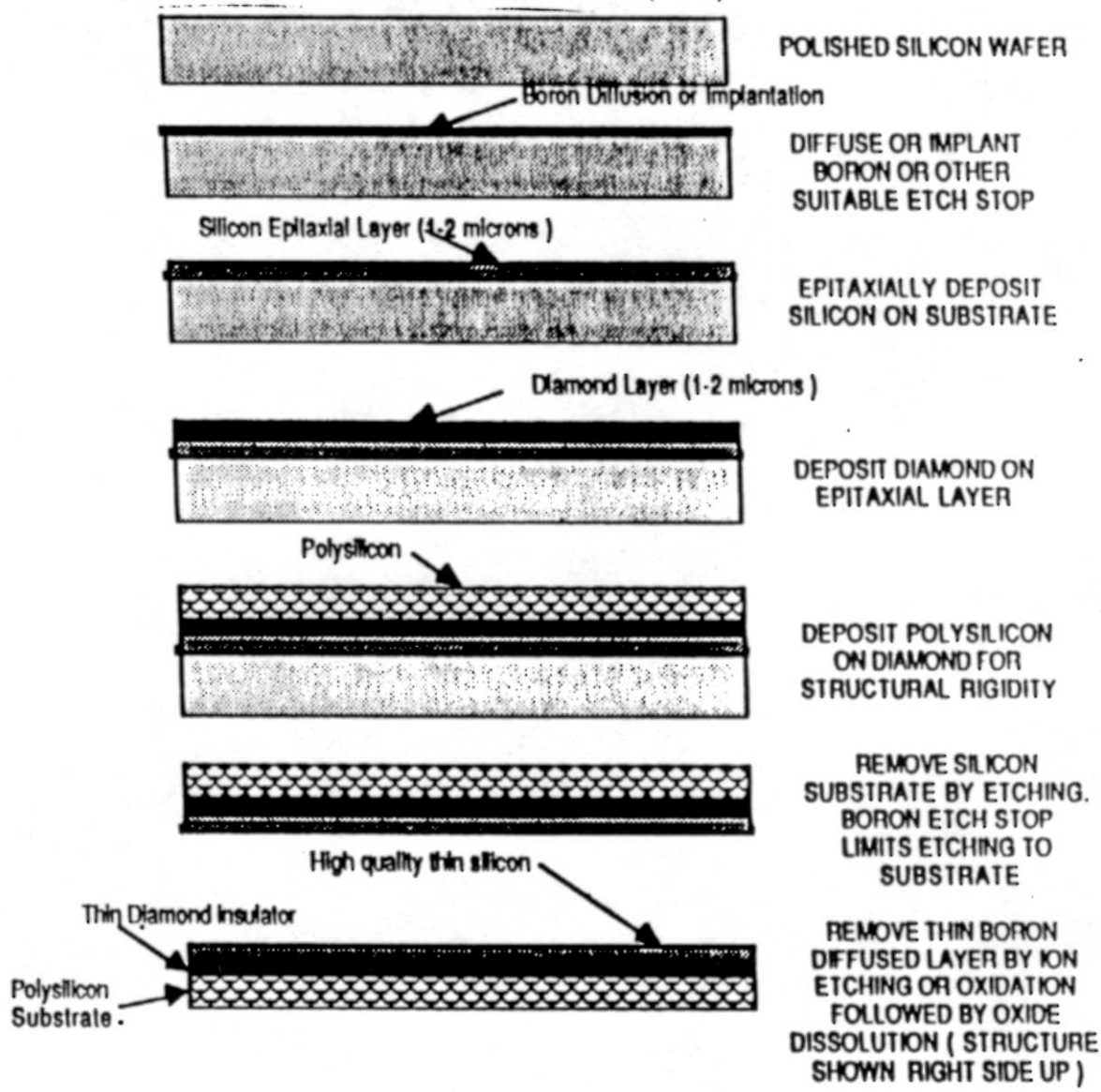


Figure 1. Schematic illustration of the process sequence for the fabrication of SOI wafers using diamond films.

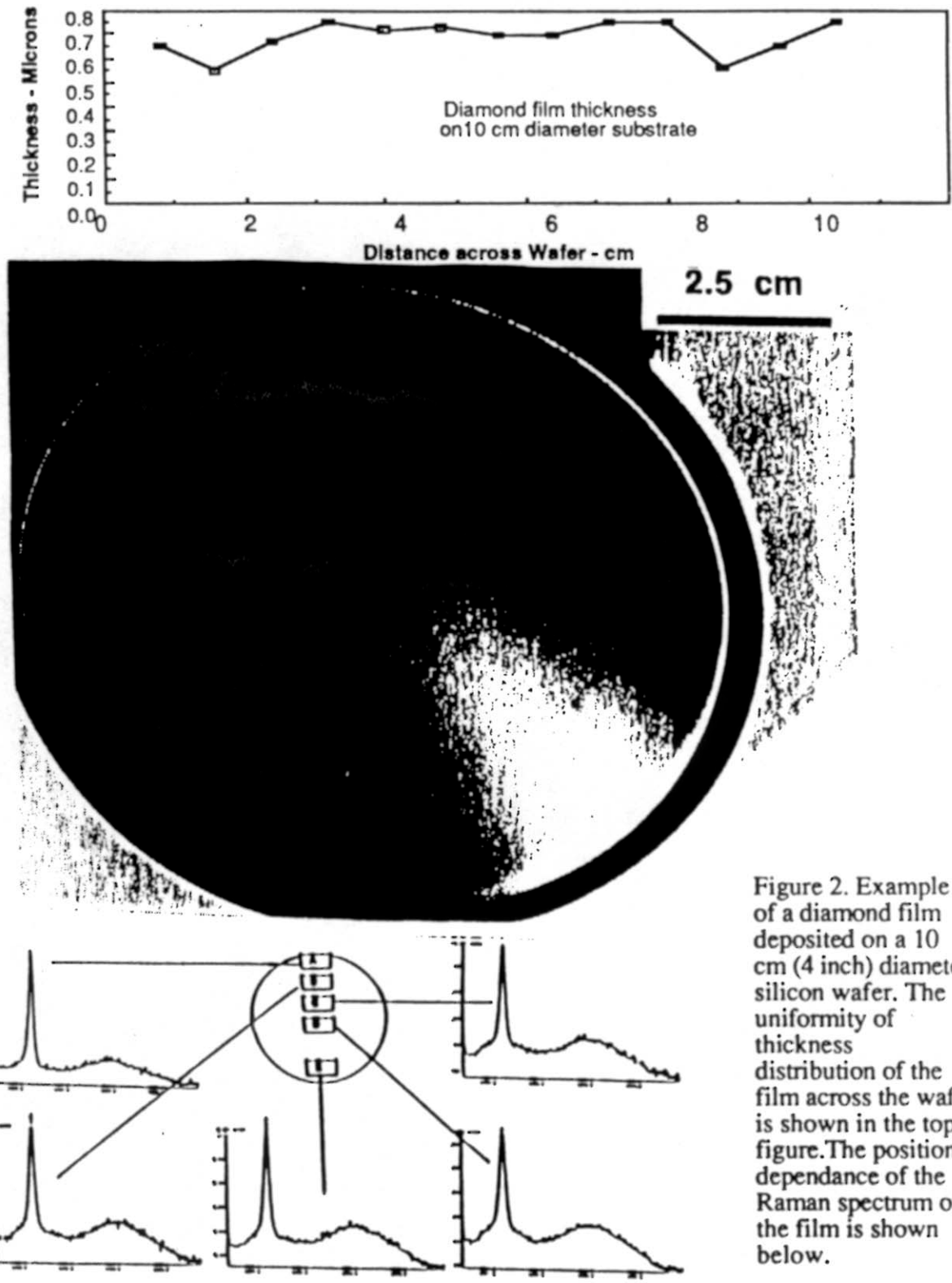


Figure 2. Example of a diamond film deposited on a 10 cm (4 inch) diameter silicon wafer. The uniformity of thickness distribution of the film across the wafer is shown in the top figure.The positional dependance of the Raman spectrum of the film is shown below.

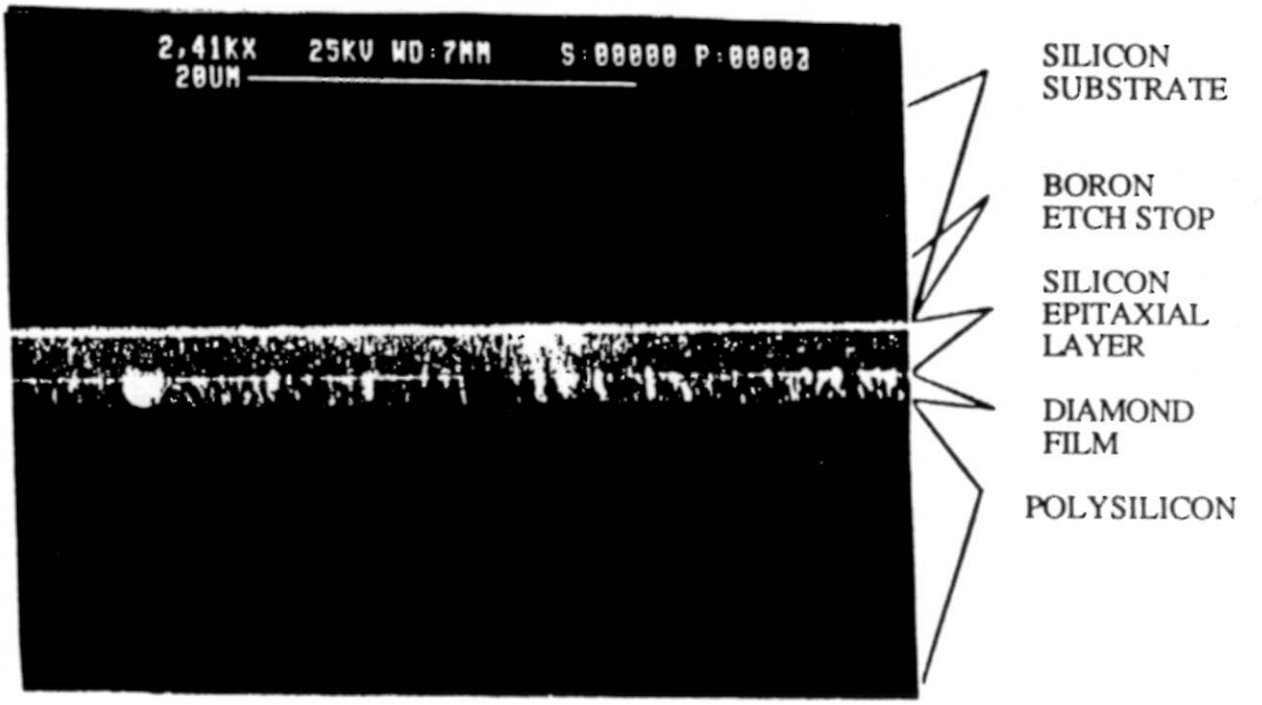


Figure 3. Cross section of structure showing the diamond film sandwitched between a silicon epitaxial layer and a polysilicon layer. The original silicon substrate with the high concentration boron etch stop is also shown

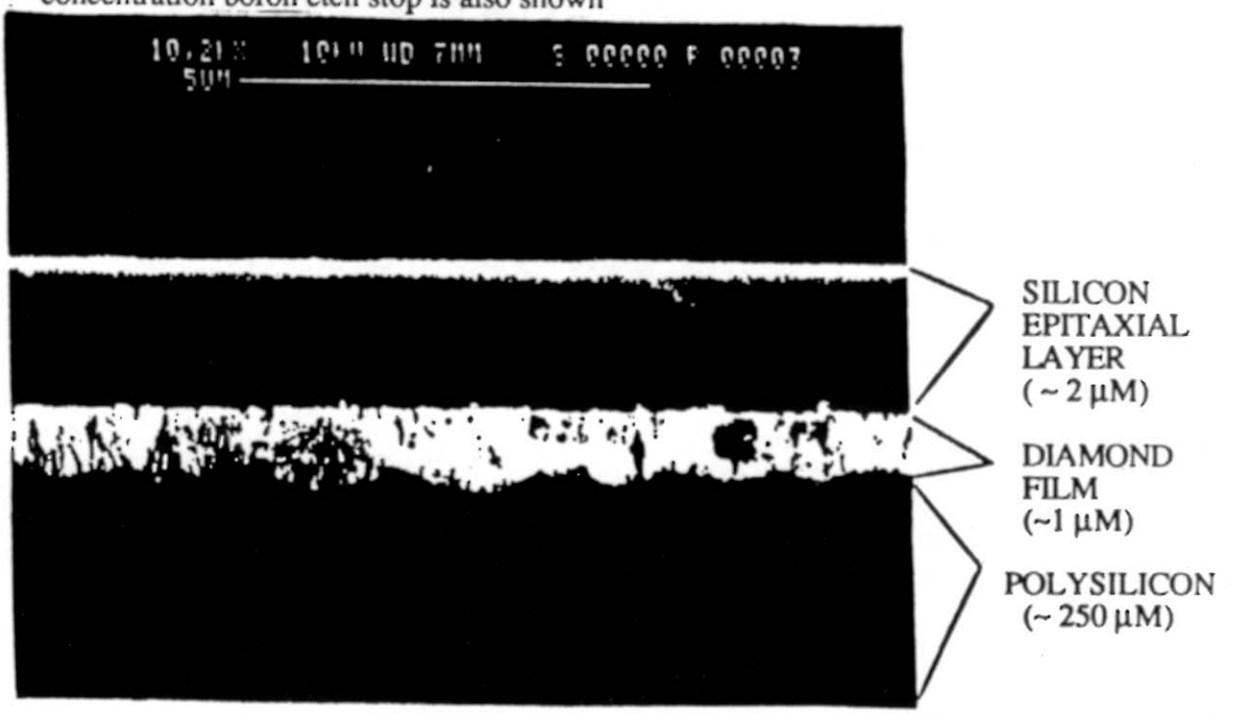
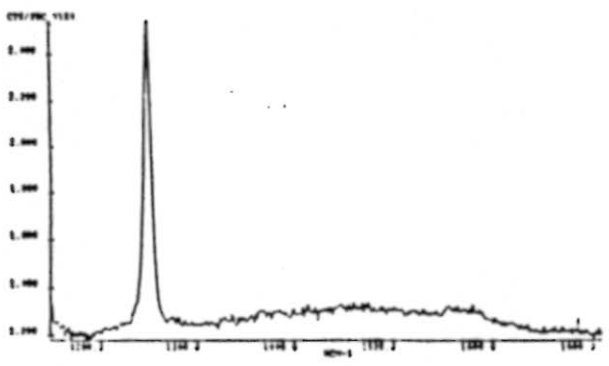
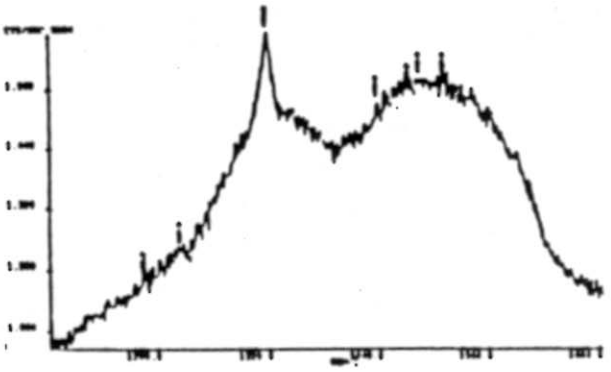


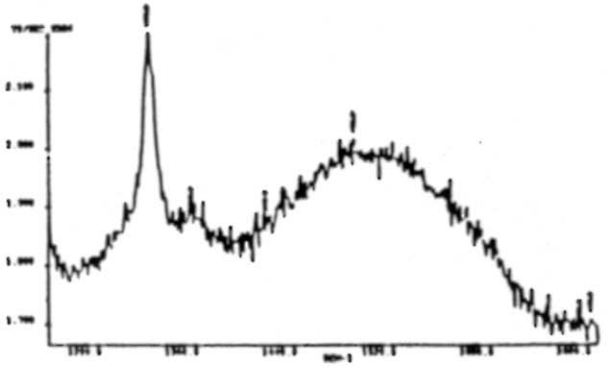
Figure 4. Cross sectional scanning electron micrograph of a cleaved section of a silicon on insulator structure using diamond. The substrate silicon has been removed by selective etching. Good planarity and stress free structures are obtained.



Resistivity - 10^5 Ohm cm



Resistivity - 10^6 Ohm cm



Resistivity - $5 * 10^{10}$ Ohm cm

Figure 5. Raman spectra and corresponding resistivity of three different diamond films. The top left spectrum is from a film synthesized using a microwave assisted plasma. The other two spectra are from films synthesized using a DC glow discharge.

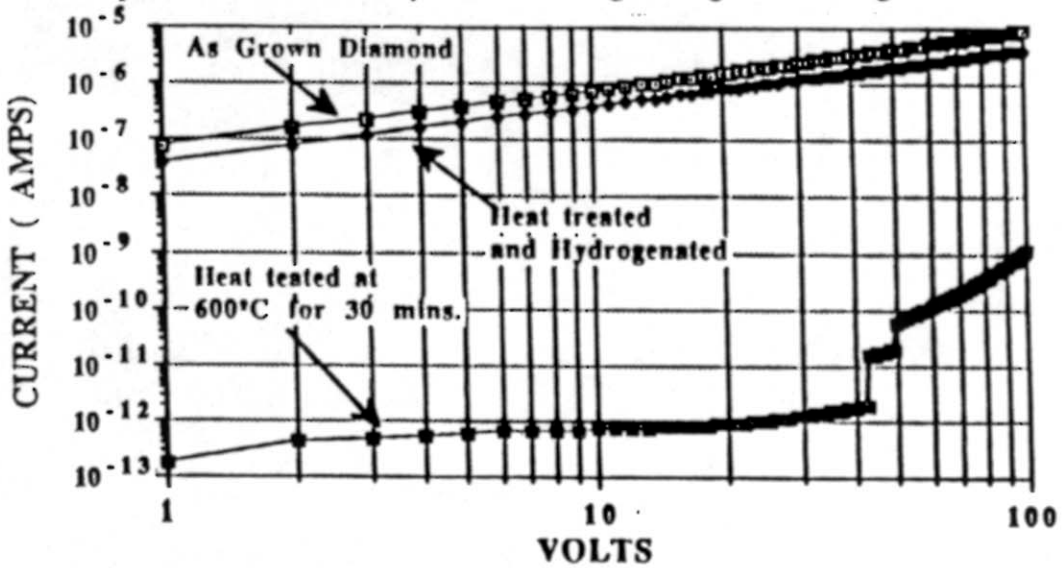


Figure 6. I-V charactreristics of a diamond film synthesized using a DC bias in the as synthesized condition and following heat treatment and rehydrogenation demonstrating the effects of hydrogen on current conduction.

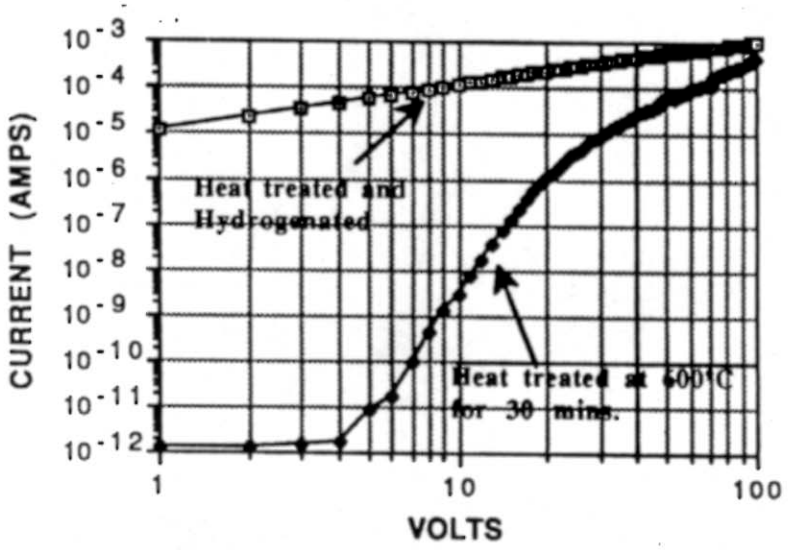


Figure 7. I-V characteristics of a diamond film synthesized using a microwave excited plasma. Current conduction characteristics of the film in the annealed and hydrogenated conditions are shown demonstrating the effects of hydrogen passivation.

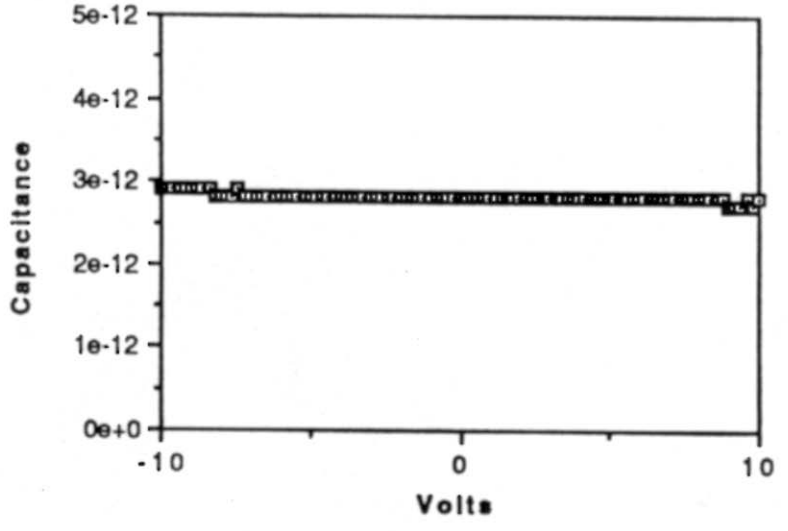


Figure 8. C-V plot of a Silicon - Diamond structure.

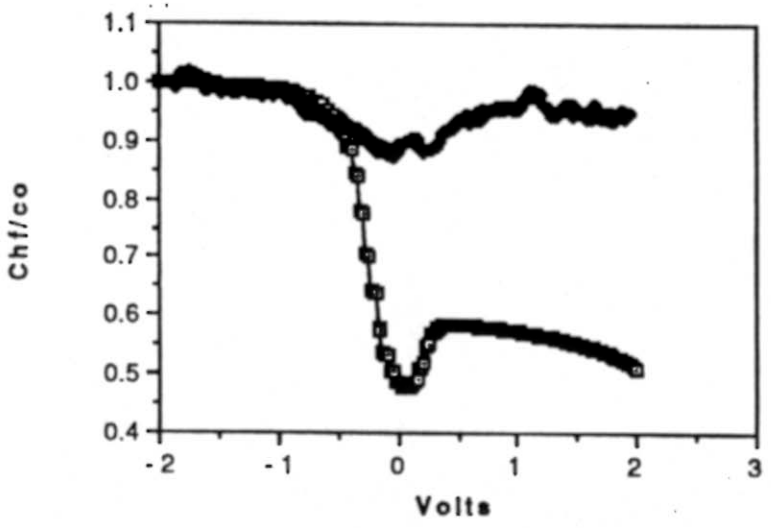


Figure 9. Frequency dependant C-V plots of a Silicon-SiO_2-Diamond structure. 100 KHz - bottom curve; 100 Hz - top curve.

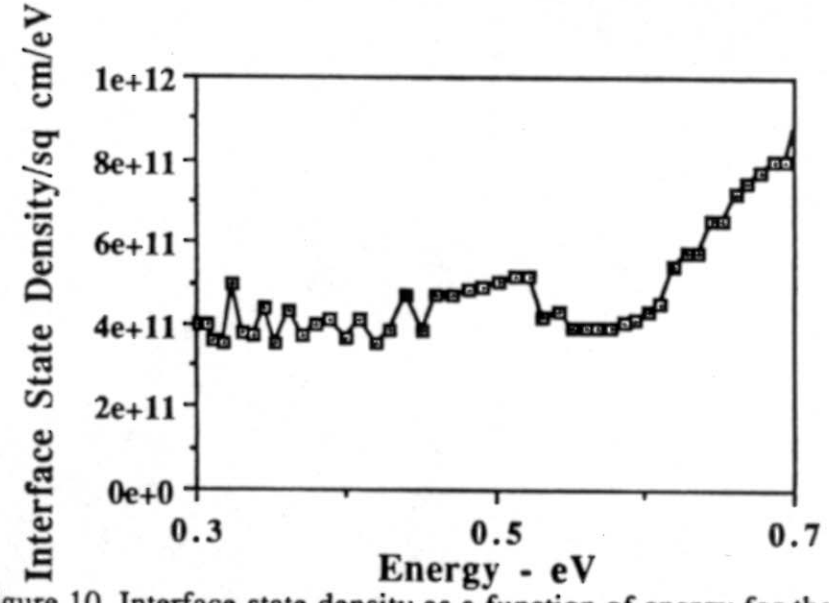


Figure 10. Interface state density as a function of energy for the Silicon-SiO_2-Diamond structure.