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GaN-on-Diamond Substrates for HEMT (High Electron Mobility Transistor) Applications

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CRYSTALLUME

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Why GaN ………..

Unlike silicon, gallium arsenide, silicon carbide and indium phosphide, only GaN can manage both high speeds and high signal purity at high power. These characteristics make GaN the ideal "super transistor."

Nitronex

………..on Diamond for HEMT

- Phenomenal thermal conductivity of diamond, for heat management
- Combine the most dynamic of III-V materials, with possibly with the most dynamic material known ~ get "super cool transistor"!

Why GaN on Diamond for HEMT

- Performance of transistors is limited by fundamental material properties.
- Power and frequency limits in analog amplification are expressed concisely with Johnson Figure-of-Merit[1] used in the industry since 1965 for relative comparison between different materials.
- The higher the JFM number the better!

For a HEMT, Johnson Figure of Merit (JFM) is proportional to the product of transit-time cutoff frequency f_t and maximum RF power $P_{\max}$ that can be delivered by the device[2].

$$JFM \equiv \left(\frac{v_S E_B}{2\pi} \right)^2 \propto P_{\max} f_t$$

E_B is breakdown electric field
v_S is the saturated drift velocity

JFM for various materials

Semiconductor	Electron mobility (cm^2/Vsec)	Relative permittivity e	Bandgap E_g (eV)	Normalized JFM Ratio
Si	1300	11.4	1.1	1
GaAs	5000	13.1	1.4	7
SiC	260	9.7	2.9	490
GaN	**1500**	**9.5**	**3.4**	**1741**

JFM for Diamond = 73856E23 $W\Omega s^2$ → 8206 times Si

[1]Max N. Yoder, "Wide Bandgap Semiconductor Materials and Devices", IEEE Transaction on Electron Devices, Vol. 43, No. 10, 1633-1636, 1996

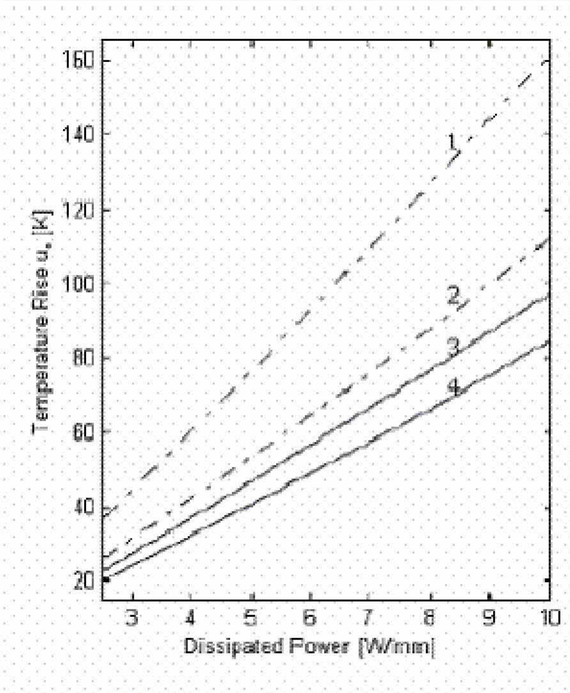
[2]E. O. Johnson, "Physical Limitation on frequency and power parameters of transistors", *RCA Review*, p. 163-177, 1965

[3]Y. F. Wu, *AlGaN/GaN Microwave Power High-Mobility Transistors*, Ph. D. Dissertation, UCSB, 1997.

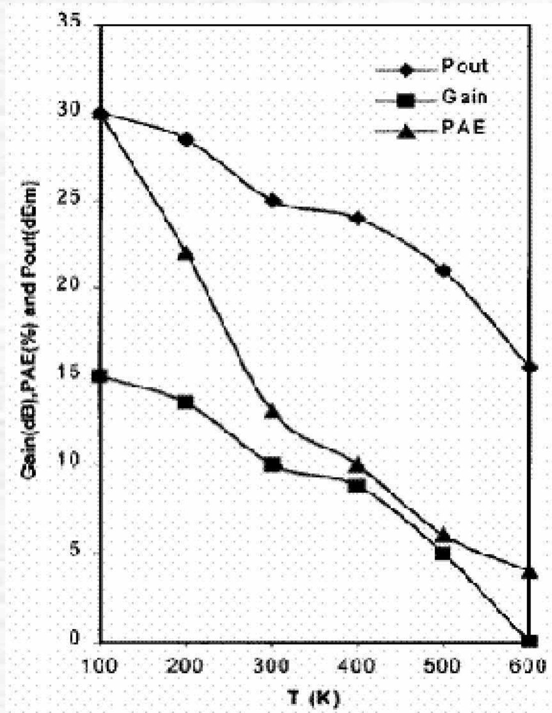
Why GaN on Diamond for HEMT

- **JFM is temperature dependent**
  - For example, when the temperature of GaN transistor is increased from room temperature to 300°C, the $P_{max}{\cdot}f_t$ product reduces by one-half.
- **JFM is an optimistic measure of transistor performance**
  - It does not account for parasitic effects, such as, ohmic resistances, field non-uniformities, and current crowding effects, all of which degrade transistor performance with increased temperature.
- **The only way to prevent degradation in performance is to reduce the thermal resistance of GaN devices.**

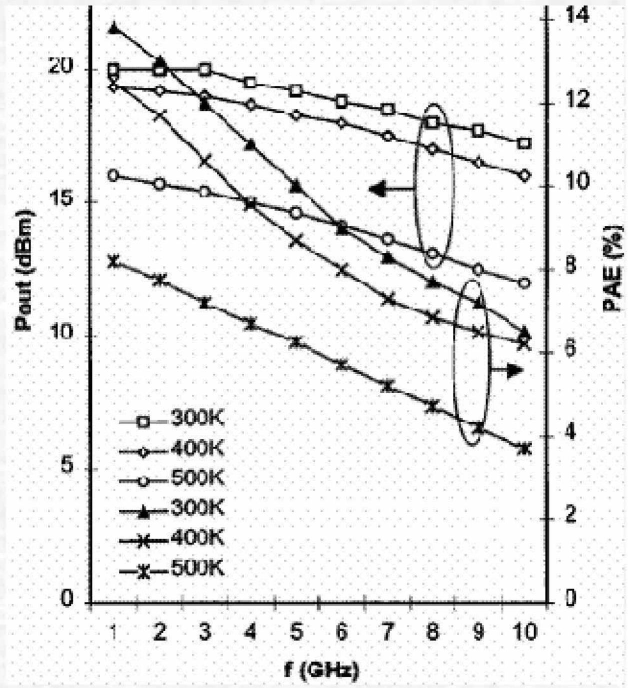
Performance Degradation with Elevated Temperature



Channel temperature increases with dissipated power

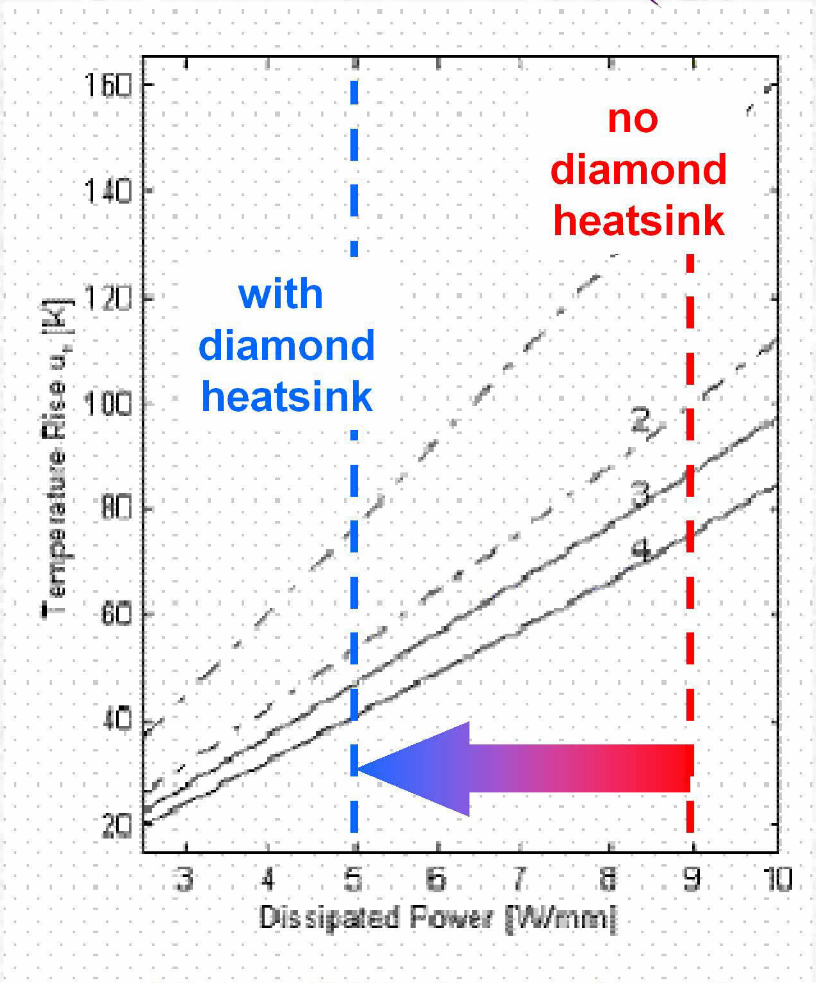


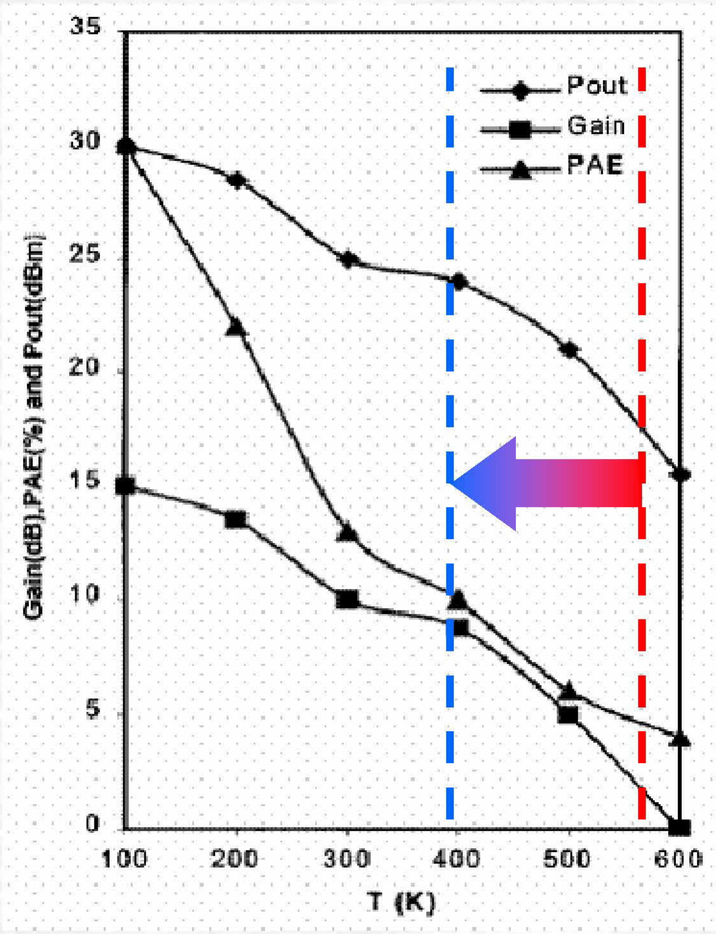
Output power and efficiency drop with temperature



Frequency response drops with temperature

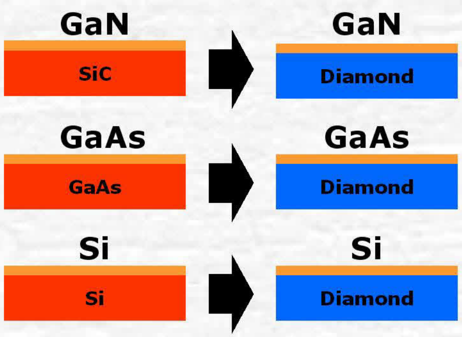
CVD Diamond Reduces Thermal Resistance (an Illustration)





Using CVD diamond as a heatsink improves the thermal resistance.
This **cools** down the device allowing higher output power
(graphical representation is qualitative)

Semiconductor-on-diamond as a new material system



(Left) An artistic depiction of how CVD diamond substrates replace traditional substrates as seed for almost all forms of electronic circuit layers.

PHYSICAL PROPERTIES OF VARIOUS SUBSTRATE MATERIALS

	Silicon	GaAs	SiC	Sapphire	CVD Diamond
Thermal Conductivity (W/m K)	135-150	35-50	399-430	35	1200-2000
Electrical Resistivity @ RT (Ωcm)	$< 2.5\times10^{3}$	$< 1\times10^{4} - 10^{7}$	$< 1\times10^{4} - 10^{6}$	$\sim 1\times 10^{17}$	$< 1\times10^{13} - 10^{16}$
Young's Modulus (110) @ RT (Gpa)	130	83	390-700	250-400	+1,100
Diameter Availability Today (near-future)	8″	4″ - 6″	3″ (4″)	2″ – 4″	4″ (8″)

Physical properties of various substrate materials; diamond is superior in its ability to efficiently conduct heat, and resist electrical conduction.

All materials would benefit from transfer to diamond substrate, the best initial candidate is GaN.

Thermal Model Structure

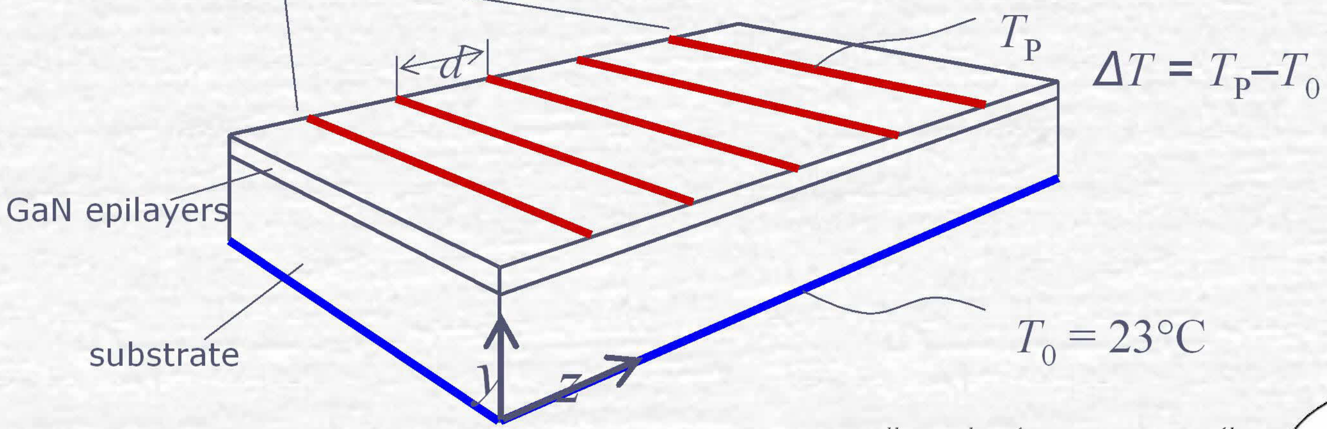
- GaN-on-Diamond ~ heat sources (embedded in GaN epilayers) within sub-micrometer proximity to high-thermally-conductive CVD diamond substrates.

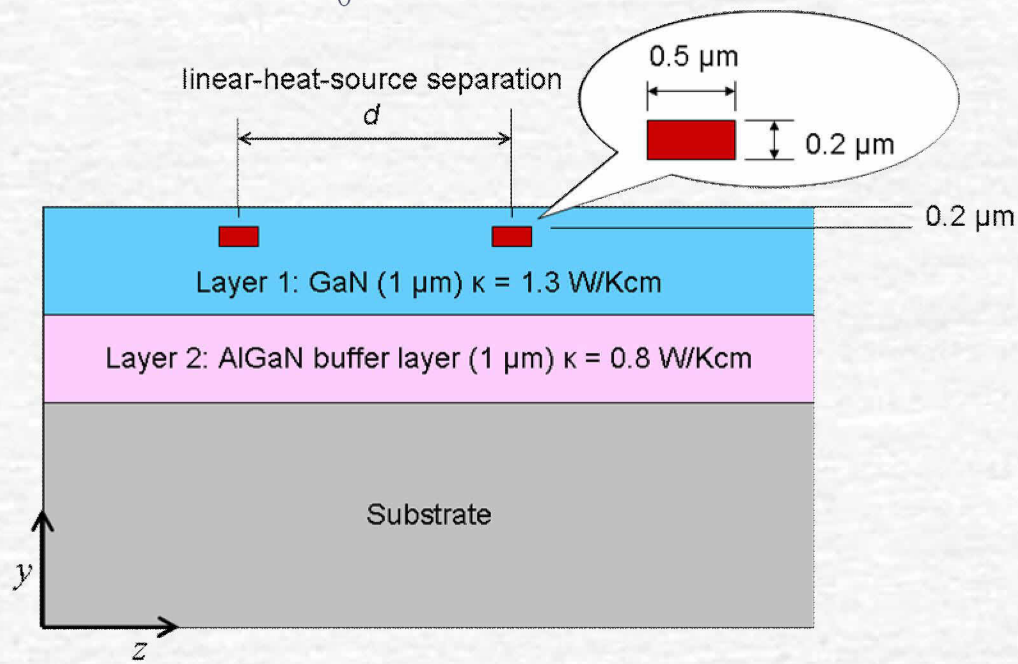
- The gates of modern high-power HEMTs are generally formed in a linear array of heat sources (gates).
  - The gate operating temperature is determined by the linear power dissipation, expressed in W/cm, the spatial separation between the gates, and the thermal conductivity of the material structure below the gate.

- The main outcome of the model is to show that one may place gates (i.e. linear heat sources) significantly closer together when CVD diamond is used as a substrate – so that the total power density per chip is amplified.

Thermal Model Structure

Array of linear heat-generating devices on GaN
(length of heat sources is long in comparison with the separation *d* and width of the sources)





Depiction of the cross-sectional view of the structure shown in above drawing

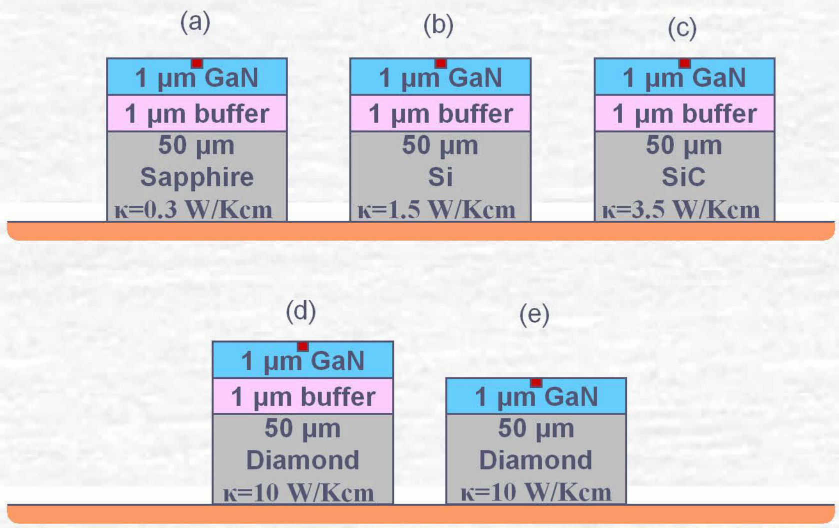
Materials Properties Assumptions

Materials	Thermal Conductivity [W/Kcm]
Si	1.49
GaAs	0.46
GaN	1.30
AlGaN Buffer average	0.80
Cu	4.01
SiO_2	0.03
SiC	3.50
CVD Diamond (C)	10.0
Sapphire	0.4

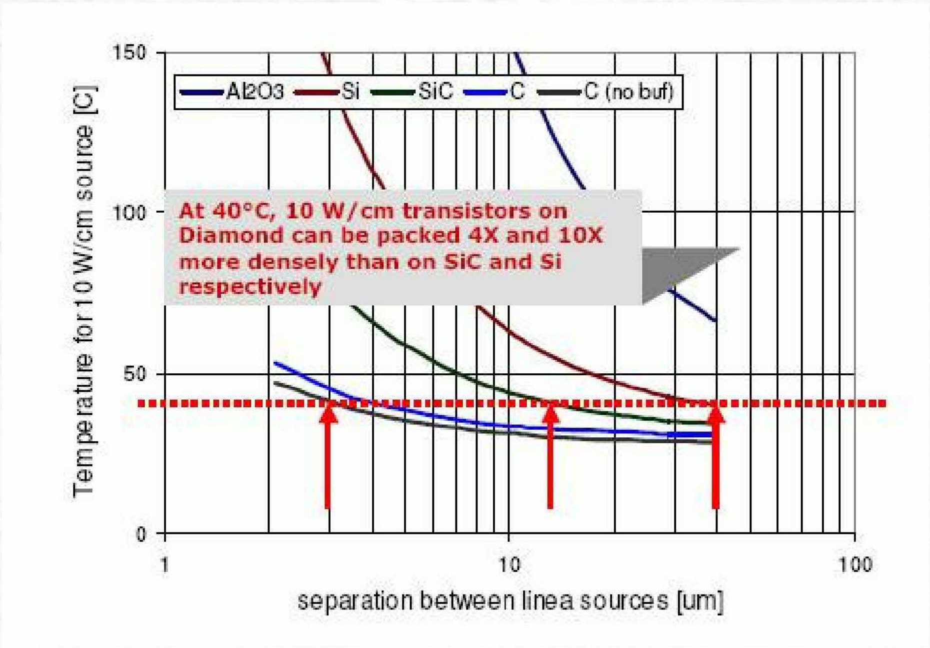
Summary of Cases Modeled

- Five structures modeled (a-e), and three different substrate thickness (1-3) for each structure
- Case 1 thru 3 (different substrate thickness) have been chosen for their typical use in the GaN industry.
- Structures (a), (b), and (c) represent industry-standard GaN structures grown directly on sapphire (Al_2O_3), silicon (Si), and silicon carbide (SiC) substrates, respectively.
- Structures (d) and (e) are gallium nitride (GaN) epilayers atomically attached to CVD diamond. Structure (d) includes diamond with a buffer layer and structure (e) has no buffer layer.
- All structures rest on a heatsink which is assumed to be at room temperature (23 ºC). The heat flow from the substrates into the heatsink is assumed uniform so that additional increases in temperature due to solders and copper heatsink thickness can be accounted for in a straightforward manner.

Substrate Thickness Case #1

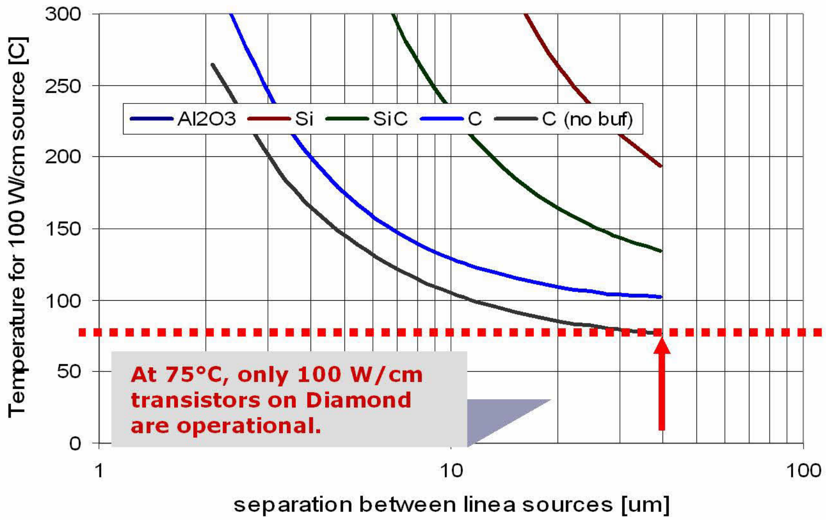


Peak (absolute) temperature assuming transistor's gate power at 10 W/cm, and the substrate's bottom at 23°C

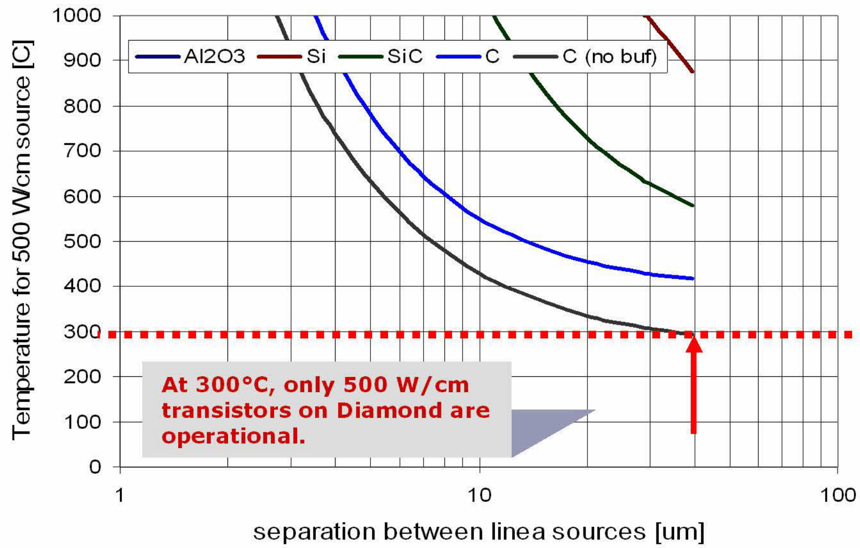


Substrate Thickness Case #1

Peak (absolute) temperature assuming transistor's gate power at 100W/cm, and the substrate's bottom at 23°C



Peak (absolute) temperature assuming transistor's gate power at 500W/cm, and the substrate's bottom at 23°C



Results Summary

Extent of power density improvement in a GaN-on-Diamond transistor compared to GaN-on-SiC transistors

CASE # 1 All substrates were assumed to be 50 microns thick.

CASE # 2 Diamond assumed to be 25 microns. Sapphire, Si and SiC were assumed to be 75 microns thick

CASE # 3 Diamond assumed to be 25 microns. Sapphire, Si and SiC were assumed to be 150 microns thick

	Case #1	**Case #2**	**Case #3**
10 W/cm devices at 40C	4X increase over GaN-on-SiC	20X increase over GaN-on-SiC	20X increase over GaN-on-SiC
100 W/cm devices at 75C	GaN-on-Diamond ⌧ GaN-on-SiC X	GaN-on-Diamond ⌧ GaN-on-SiC X	GaN-on-Diamond ⌧ GaN-on-SiC X
500 W/cm devices at 300C	GaN-on-Diamond ⌧ GaN-on-SiC X	GaN-on-Diamond ⌧ GaN-on-SiC X	GaN-on-Diamond ⌧ GaN-on-SiC X

Why GaN on Diamond for HEMT

- Placing GaN HEMT on top of CVD diamond reduces the device thermal resistance.
- This means at given frequency and given ambient temperature, more power can be extracted from the device.
- Is there a fundamental limit beyond which reducing the thermal resistance offers no improvements?
  - Answer: There is a material-related fundamental limit to the power and frequency performance of transistors (JFM). That limit is higher for lower temperatures. Namely, lowering thermal resistance of a transistor, which keeps the transistor operating at a lower temperature, **always** helps its power and frequency capability.

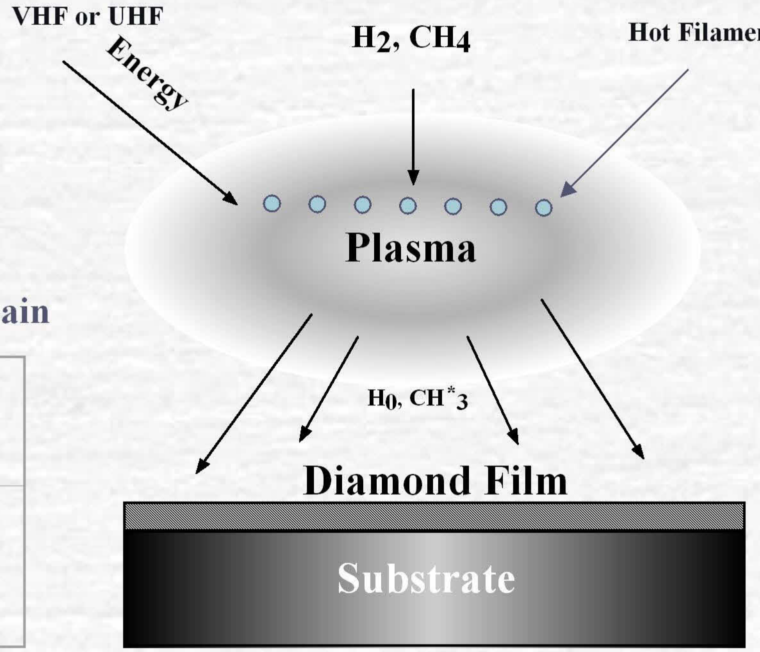
Generic Diamond CVD

- Requires short-lived excited species: H^0, CH^*_3
- Chemistry requires high pressure (> 20 Torr for commercial use)

List and range of the factors used to map the deposition domain

Gases	Pressure	Tempera ture	Power Density	CH4/H2 Ratio
H2/CH4/ O2	30-100 Torr	700-900 ⁰C	400-800 Watts/in 2	2% to 4%

Diamond CVD Process



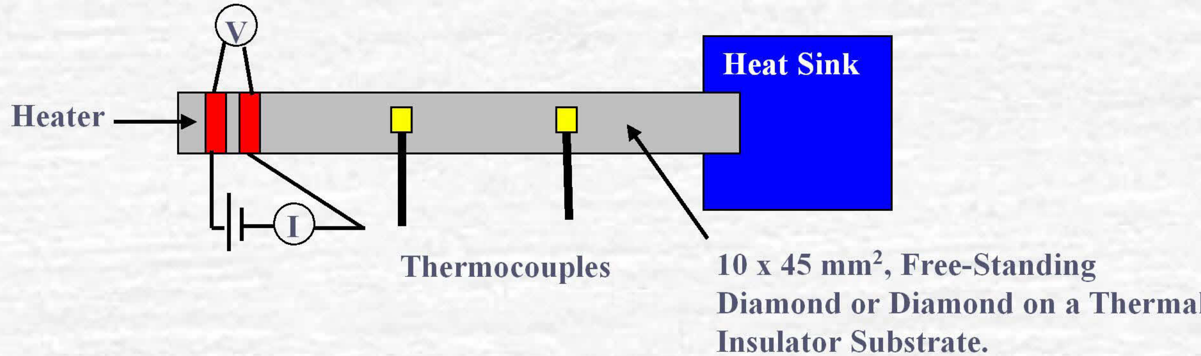
Reactants made remotely, diffuse to growth region

Diamond Properties

Property	Value	Comments
Chemical Reactivity	Extremely Low	
Hardness (GPa)	80 - 100	CBN: 50, SiC: 40
Thermal Conductivity (W/cm·K)	**8-10**	**Ag: 4.3, Cu: 4.0, BeO: 2.2**
Fracture Toughness (MPa/√m)	5.5	SiO_2: 1, SiC: 4, Al_2O_3: 4
Young's Modulus (GPa)	**1050**	**SiC: 440, Graphite: 9**
Thermal Expansion Coeff. (K^{-1})	**1.2×10^{-6}**	**SiO_2: 0.5×10^{-6}**
Refractive Index	2.41 @ 590 nm	Glass: 1.4 - 1.8
Transmissivity	225 nm - far IR	Widest known
Coeff. of Friction	0.05 - 0.1 (in air)	Teflon: 0.05
Band Gap (eV)	5.4	Si: 1.10, GaAs: 1.43
Electrical Resistivity (Ω-cm)	**10^{12} -10^{16}**	**AlN: 10^{14}, Al_2O_3: 10^{15}**
Density (gm/cm^3)	3.51	Si: 2.32, Cu: 8.89

Whilst the thermal conductivity of typical CVD diamond is about 2.5 X better tha copper, the thermal diffusivity is about 4 X better ➔ diamond is a far superior heat-spreader

Thermal Conductivity of Diamond CVD



Measured thermal conductivity of diamond

20 microns Diamond on Strip	CH4/H2 = 2%	883 Watts/meter. ⊕K
50 microns Diamond on Strip	CH4/H2 = 2%	922 Watts/meter. ⊕K
20 microns Diamond on Strip	CH4/H2 = 3.5%	761 Watts/meter. ⊕K
400 microns Free-Standing Diamond	CH4/H2 = 2%	940 Watts/meter. ⊕K

Stress of Diamond CVD

Measured Stress for SoD and freestanding diamond

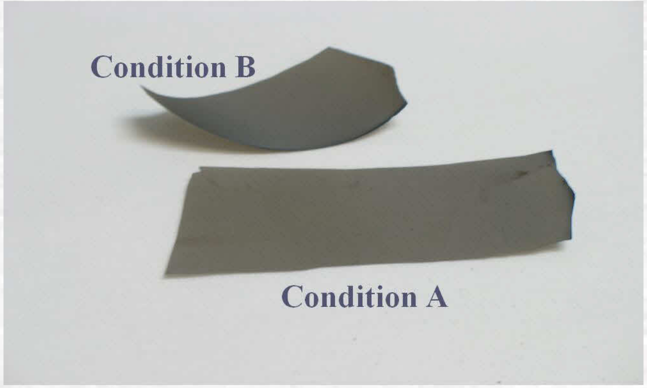
Process	Diamond-on-Silicon	Free-Standing Diamond
Condition A	2.29E+09 dyn/cm2 compressive	7.65E+07 dyn/cm2 tensile
Condition B	4.64E+09 dyn/cm2 tensile	6.94E+09 dyn/cm2 tensile

Calculated the intrinsic stress:

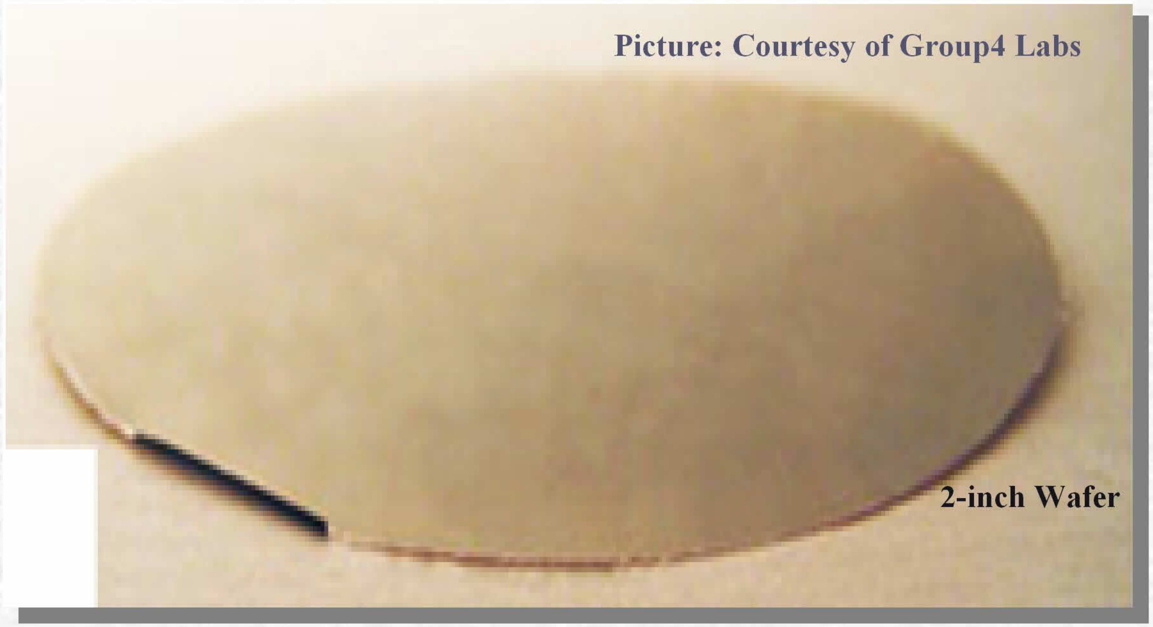
♦$_T$ = ♎/r^2 * E/3(1-■) * d^2_s/d$_f$ (Stoney Equation)

♦$_T$ = ♦$_{thermal}$ + ♦$_{intrinsic}$

♦$_{thermal}$ = E$_f$/(1-■) * (♋$_f$ - ♋$_s$) * (T$_{dep}$ – T$_m$)

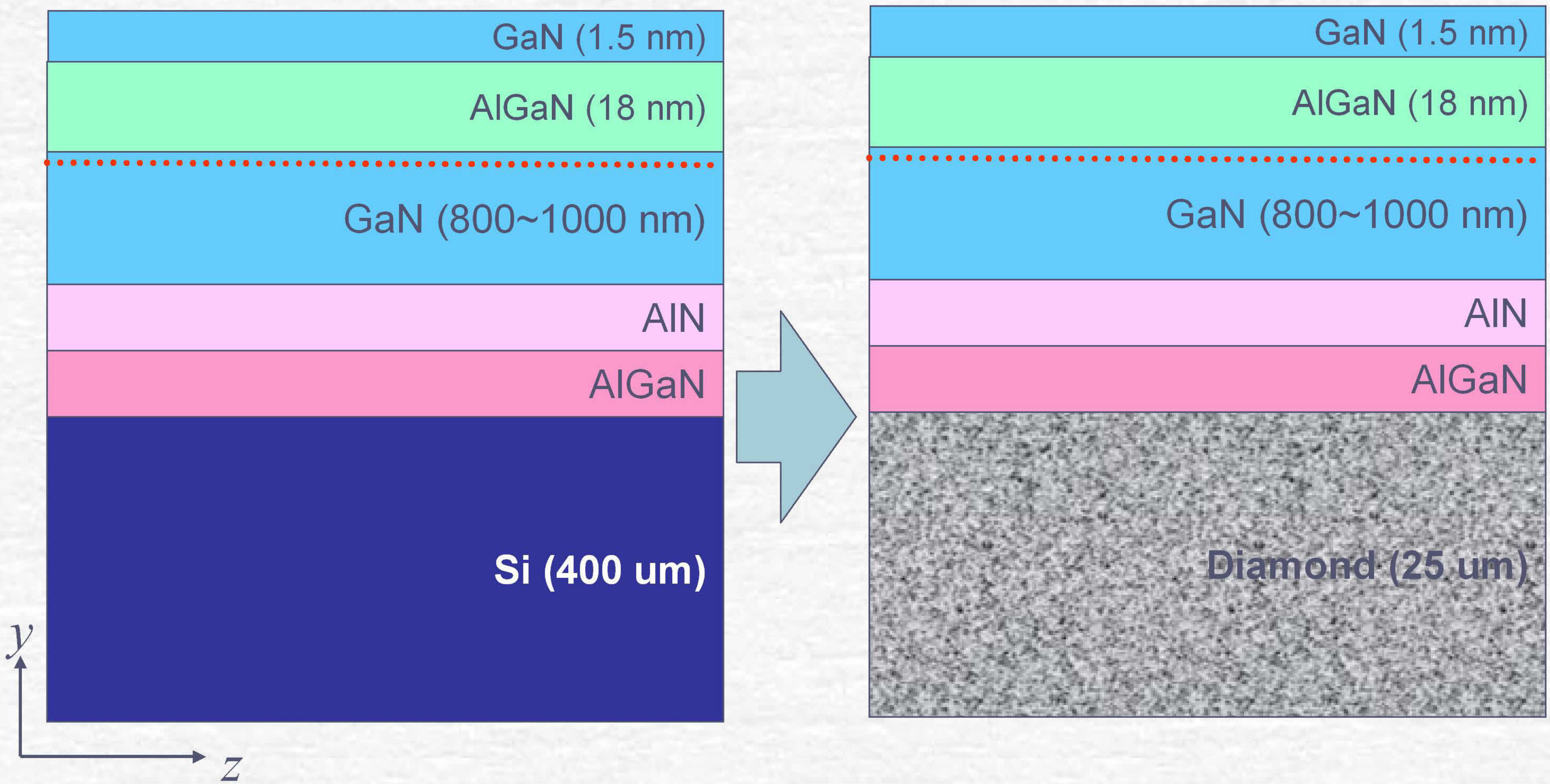


Stress of Diamond CVD



- On-going work on 4-inch (100mm) Wafer
- Process is characterized for 2” (50mm) wafer
- Major hurdle is handling!

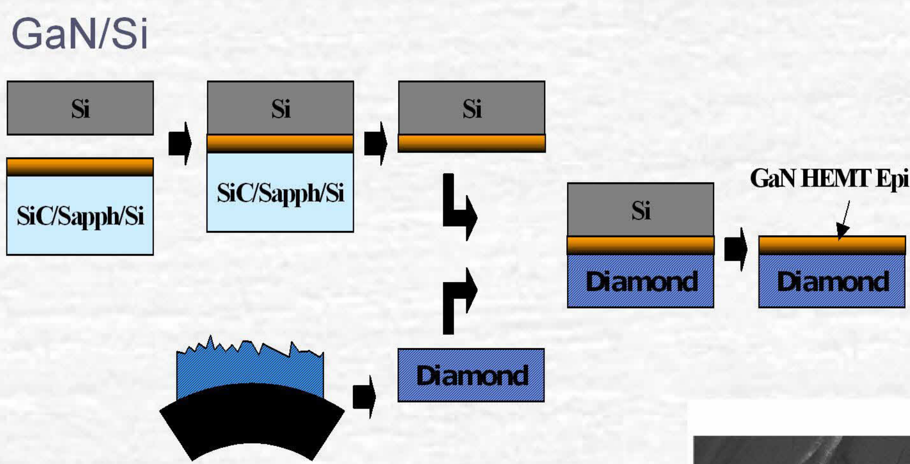
Epitaxial GaN transfer

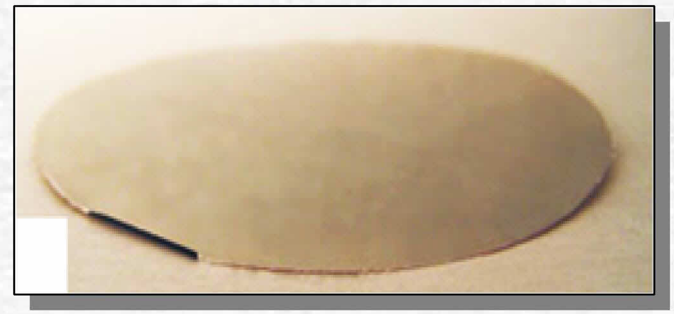


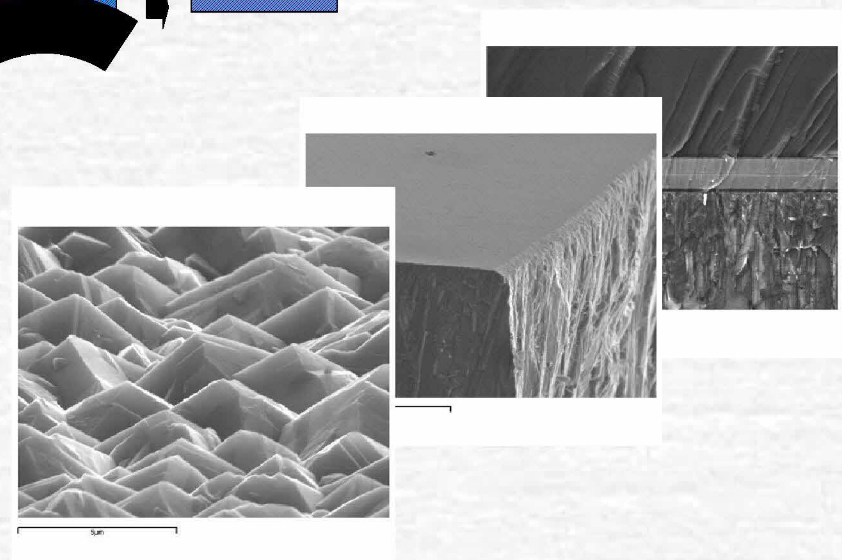
To get electronic devices to work we need to transfer epi where the top 20nm are the active layers.

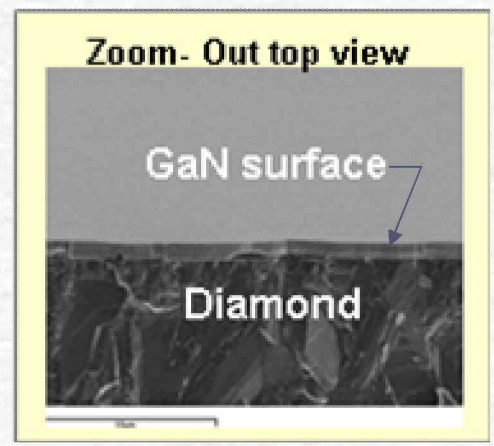
Courtesy of Group4 Labs

GaN-on-Diamond Process







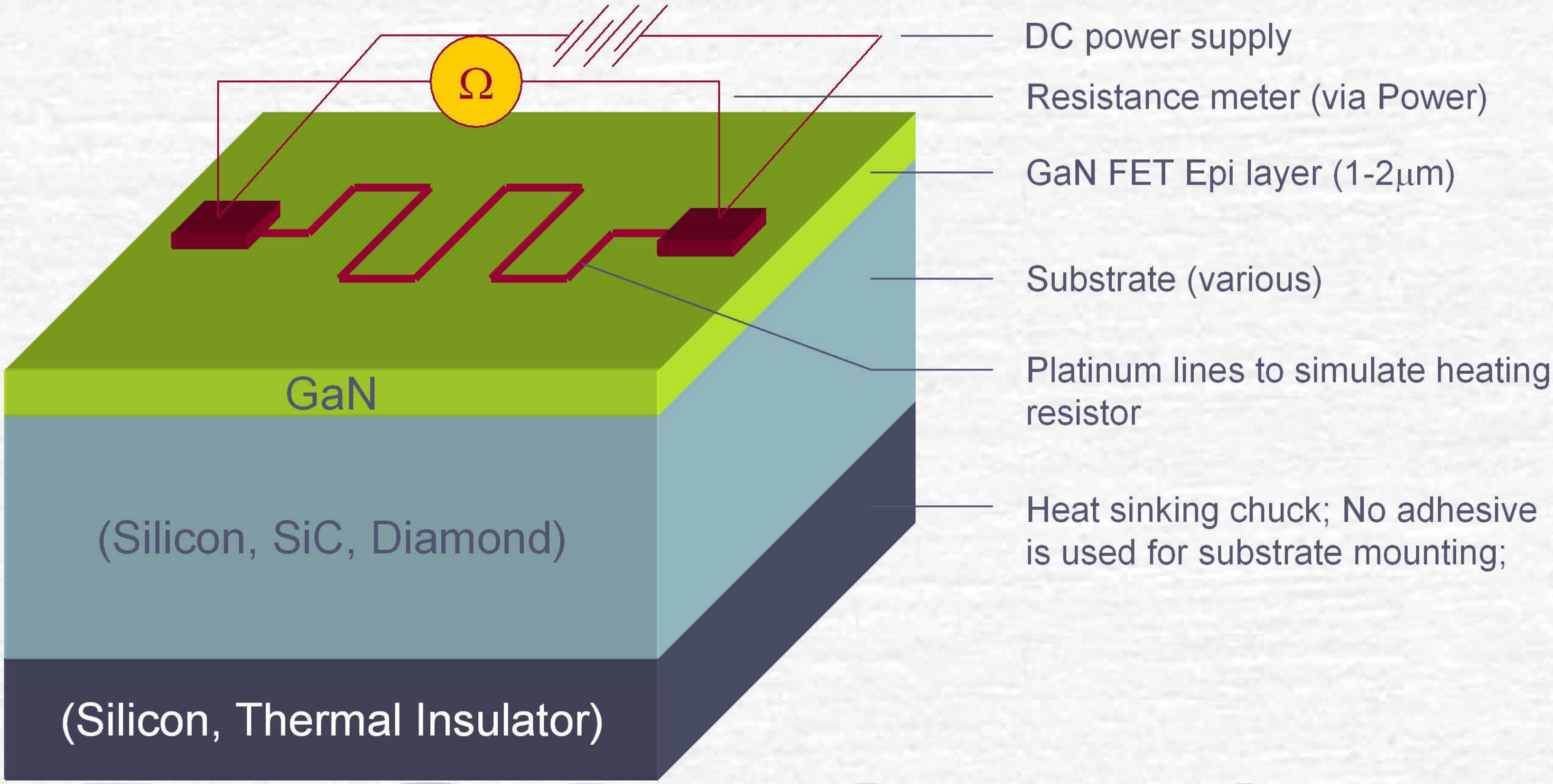


Result is GaN atomically attached to diamond

DC Resistor Testing

A resistor-based experiment was devised to i) generate FET-like power on a GaN-on-Diamond wafer surface, and ii) measure surface temperature changes associated with the power.

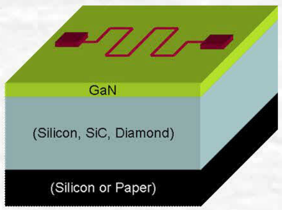
RESISTOR EXPERIMENT SETUP



Courtesy of Group4 Labs

Resistor Experiment Setup

Platinum resistors were designed to mimic typical FET-power levels used in traditional commercial applications.

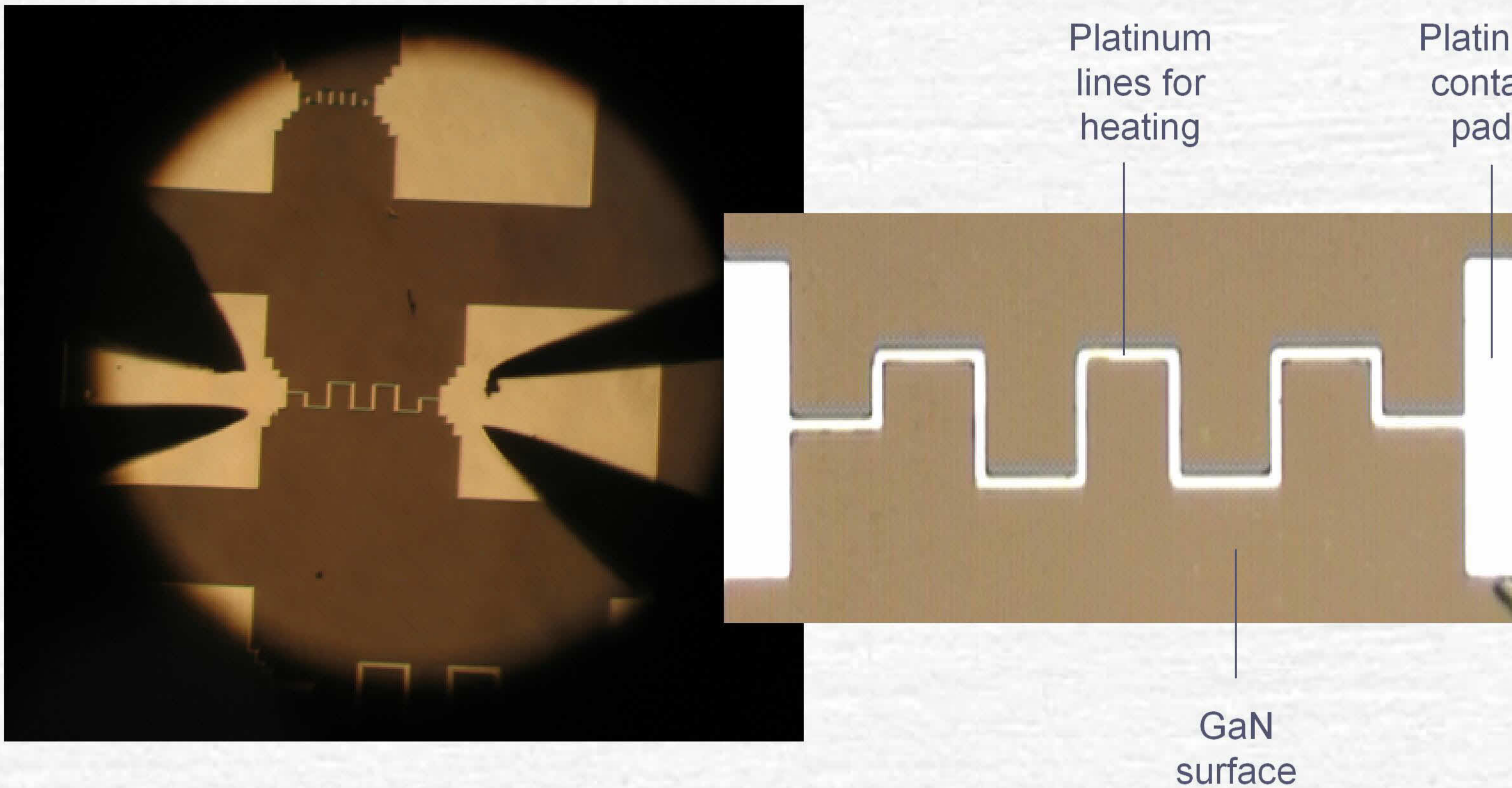


MEASUREMENT OBJECTIVE	A standard 4-point probe measurement scheme was used to measure the resistance of the platinum resistor while the resistor's temperature was steadily increased via rising current.	
Platinum Resistor Dimensions	Total Line Length: Line Width: Area:	300-1500 μm 5 - 25 μm $2\text{-}8 \times 10^{-4}$ cm^2
GaN Layer	GaN layer thickness:	2-μm
Substrate Thickness	SiC substrate thickness: Diamond thickness: Si thickness:	400-μm 25-μm 525-μm
Heat Sink	Silicon & Paper	
Test Conditions	Power density range: Adhesion to heat-sink:	500 – 2200 W/cm^2 Free-standing

Courtesy of Group4 Labs

Platinum Resistors On GaN-on-Diamond

Excellent quality platinum resistor lines were fabricated atop the GaN-on-Diamond wafers.

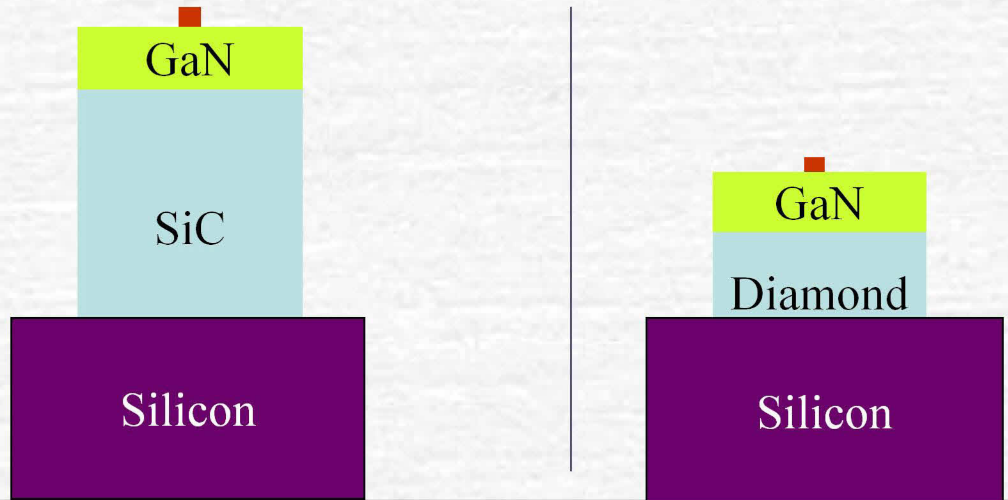


Courtesy of Group4 Labs

DC Resistor Testing

Resistor results measured as-yet show a temperature reduction of nearly two-fold in GaN-on-Diamond compared to GaN-on-SiC; better heat-sinking could reduce the thermal impedance even further in the diamond scenario

Partial Resistor Results



Substrate Thermal Conductivity	**400 W/m/K**	**1,000 W/m/K**
Resistor Area	**6000 ❍m^2**	**6000 μm^2**
Power Density	**498 W/cm^2**	**1560 W/cm^2**
Measured Thermal Impedance	**40°C/W**	**17°C/W**

GaN-on-Diamond FET DC data

Measured GaN-on-Diamond FET data	Vendor-1	Vendor-2
Sheet resistivity (Lehighton)	420 Ω/□	385 Ω/□
Drain-Source current I(sat-max)	1000 mA/mm	1200 mA/mm
Contact resistance	0.50 Ω-mm	0.52 Ω-mm

SELECTED PUBLISHED GaN FET-on-SiC REFERENCES

IEEE ELECTRON DEVICE LETTERS, VOL. 25, NO. 7, JULY 2004 459

12 W/mm AlGaN–GaN HFETs on Silicon Substrates

J. W. Johnson, *Member, IEEE*, E. L. Piner, A. Vescan, *Member, IEEE*, R. Therrien, P. Rajagopal, J. C. Roberts, *Member, IEEE*, J. D. Brown, *Member, IEEE*, S. Singhal, and K. J. Linthicum

- I_{ds} = 1040 +/- 40 mA/mm
- Source resistance = 0.86 Ohm/mm
- 2DEG = 310 Ohms/sq

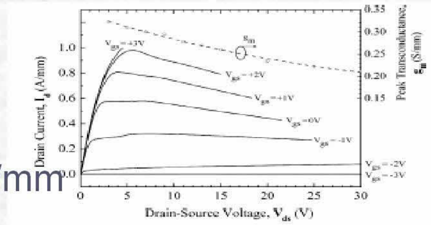


Fig. 2. Output characteristics of 100-μm gate width AlGaN–GaN HFET illustrating 1 A/mm drain current density. Also shown is extrinsic transconductance as a function of V_{ds} with peak g_m of 325 mS/mm. Transconductance of >200 mS/mm is maintained beyond V_{ds} = 30 V.

616 IEEE ELECTRON DEVICE LETTERS, VOL. 24, NO. 10, OCTOBER 2003

AlGaN–GaN HEMTs on SiC With CW Power Performance of >4 W/mm and 23% PAE at 35 GHz

Cathy Lee, Paul Saunier, Jinwei Yang, and M. Asif Khan

- I_{ds} = 1200 mA/mm
- R = 325 Ohm/sq
- Contact resistance = 0.57 Ohm/mm

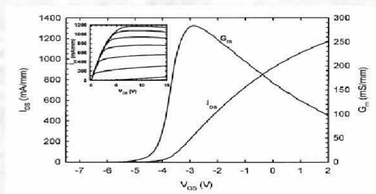


Fig. 1. DC transfer characteristics of a 200-μm AlGaN–GaN HEMT. The drain bias was 10 V. Inset: dc drain current–voltage characteristics where V_{GS} = 2 to -5 V.

Results Summary

- 2” GaN-on-Diamond template wafers were demonstrated
- 2” FET-on-Diamond wafers were demonstrated
- Handling and flatness are most critical in fabrication of of GaN FET-on-Diamond wafers.
- GaN-on-Diamond resistors were fabricated; Results were in good agreement with the model.
- Resistor testing showed that junction temperatures are critically dependent on proper heat spreading of the fabricated device.

Additional Results Beyond DC Testing

- GaN-on-Diamond FET devices were recently demonstrated for the first time at AFRL and Cornel University
  - "AlGaN/GaN HEMT on Diamond Technology Demonstration", Jenssen, G. H. et al, Compound Semiconductor Integrated Circuit Systems, Nov. 2006 IEEE, Pages 271-274
  - "Fabrication & Characterization of GaN-on-Diamond HEMTS", Felbinger, J. et al, Workshop on Compound Semiconductor Materials and Devices (WOCSMMAD), 2007 Savanah, Ga