GaN-on-Diamond substrates for HEMT applications

*This paper by, **F. N. Faili, C. Engdahl** and **E. Francis**, presents an updated overview of the latest development in hot filament assisted CVD diamond growth and diamond integration with electronic materials. In this investigation, we study the successful demonstration of GaN on diamond and review and compare the results with that of silicon on diamond (SOD). The effects of process conditions on the characteristics such as stress and thermal conductivity are described. The as-deposited diamond films were characterised by stress and morphology. The GaN on diamond stack were evaluated optically and electrically. A steady-state technique was used to measure the thermal conductivity of the deposited and free standing diamond and the GaN/Diamond layers.*

GaN-on-Diamond wafers are intended for use in high power GaN transistors typically deployed for military applications and commercial cellular base stations. This paper describes recent progress towards manufacturing robust commercial-grade products, along with recent resistor measurements.

Currently, the performance of X-band devices is thermally limited [1-3] and would benefit from highly efficient heat extraction. Devices fabricated on GaN-on-Diamond wafers have the potential for highly efficient heat extraction compared to those GaN devices fabricated on sapphire, Si or Silicon Carbide (SiC) wafers. This benefit is due to diamond's exceptional thermal conductivity (800-1200 W/m/K).

In our proprietary process, we lift-off GaN FET epi from the host substrate (e.g. Si) and atomically attach it to a polycrystalline CVD diamond substrate. First, the GaN epi is bonded face down to a temporary carrier wafer. Second, the host substrate is etched off using either a wet chemical or dry etch process that is selective to GaN, and the exposed GaN epi backside is specially treated with a nanometer-thin dielectric coating. Finally, the diamond substrate is atomically attached using a proprietary process where the first layer of diamond atoms chemically bonds with the backside of the specially treated GaN epi. We transfer fully formed GaN epitaxial layers (epi) to a carefully prepared CVD diamond substrate so that a state-of-the-art GaN epi remains state-of-the-art.

The sheet and contact resistance results are virtually identical to many published reports of industrial GaN on either Si or SiC, indicating a GaN material that is unchanged during the epitaxial transfer process. The preliminary transistor data indicates a non-affected 2D electron-gas capable of achieving transistor function. Challenging issues pertaining to wafer bow, and thermal conductivity are also presented in the paper.

Simulation model

A simple two-dimensional, numerical model for thermal simulation, was developed to further investigate the potentials of GaN-on-Diamond and compare the results with other available GaN-on-Substrate structures. Figs 1 and 2 are the representation of the generic structure that was evaluated using finite element analysis.

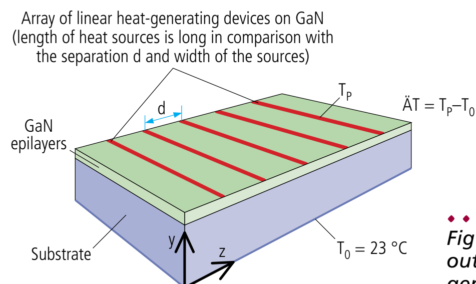


Fig 1 3-dimensional outline of the general structure

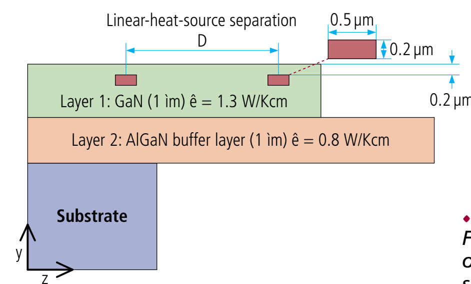


Fig 2 Frontal view of the assumed structure

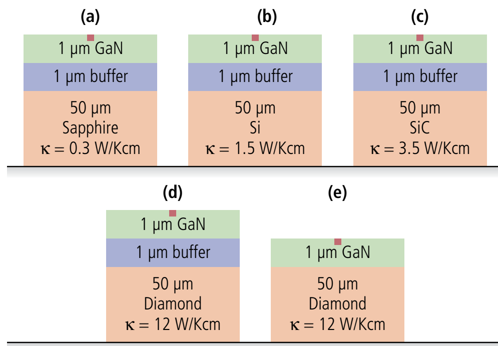


Fig 3 Five different GaN-on-Substrate structures evaluated by the thermal simulation

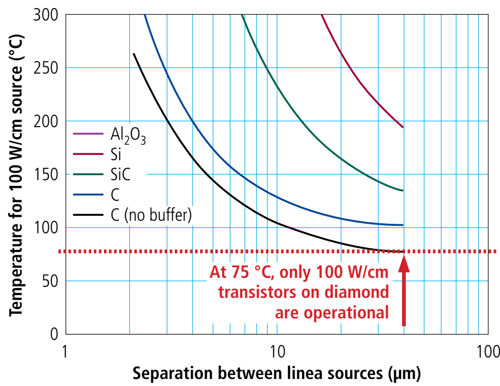


Fig 4 Junction temperature for various structure @ variable power density

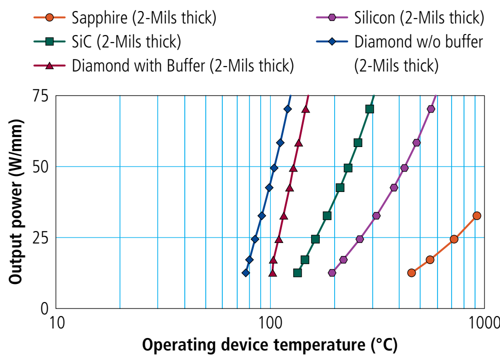


Fig 5 Operating device temperature for various structures

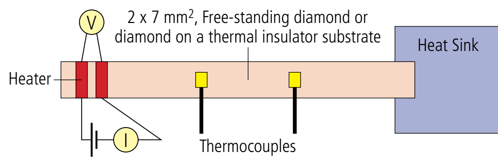


Fig 6 Top view of the sample and the test set-up

It was assumed that each chip had a fixed length (L) of 3 mm. The gate length (W) was assumed to be 150-microns. It was further assumed that the carrier beneath the substrates is infinite and is a perfect thermal conductor. The chip power density presented here, is defined as Watts per Area (L*W) given a device's (active junction) maximum allowable operating temperature.

As represented in Fig 3, five different structures were highlighted as cases a, b, c, d, and e and were evaluated, using the simulation.

Fig 4 shows, that with an assumed gate input power of 10 W/mm and the substrate's bottom temperature maintained at 23 °C, diamond could reduce the pitch to 10-mm, and still see the temperature drop of 100 °C compared to SiC.

The simulation also shows (Fig 5), that for an assumed gate to gate pitch of 50 microns for GaN-on-Diamond, one could expect the GaN junction temperature to drop by almost 100 °C.

Simply put, the simulation highlights the expected great potential of GaN-on-Diamond with significant impact on the design rules and the junction temperature.

Diamond layer

Diamond was deposited using hot-filament CVD process [4-6]. The material was grown in both single-wafer, as well as 4-wafers batch reactors. An RSM (Response Surface Methodology) model was used to map the diamond growth regime. Table 1, contains the list and range of factors varied to study the response various characteristics variables.

The two most significant characteristics evaluated, were the thermal conductivity of thin diamond film and the state of the stress of the free-standing diamond layer.

Thermal conductivity

Clearly the most significant property of the diamond for GaN-on-Diamond is its thermal conductivity. The in-plane thermal conductivity of the deposited polycrystalline diamond was measured using Joule heating thermometry [7]. Strips of free-standing diamond and diamond deposited on strips of thermal insulator (Fig 6) were laser-cut and used for measurement of thermal conductivity.

The set-up was calibrated by measuring the thermal conductivities of known copper and silicon specimens. Table 2 presents some of the highlights of the measured thermal conductivities for different diamond layers as well as free-standing diamond films.

Stress

The second most significant property of diamond for this application is film stress. However, unlike the needs for the Silicon-on-Diamond (SoD), in this case the state of flatness of the released (free-standing) diamond film is as important as the over-all diamond on silicon substrate flatness.

A series of test was done to establish the level and direction of stress in diamond. The total stress for the Diamond-on-Silicon stack was measured using Glang et el. [8, 9] version of Stoney's formula.

$$\sigma = \delta/r^2 * E/3(1-\nu) * d_s^2/d_f$$

where δ = wafer deflection in cm, r = radius of the scan, E = Young's modulus of Si substrate (1.33 x 10^{12} dym/cm^2), ν = Poisson coefficient for Si (~ 0.28), d_s = thickness of substrate (0.055 cm to 0.300 cm), d_f = thickness of the diamond film, and σ = film stress in dyn/cm^2.

Gases	Pressure	Temperature	Power Density	CH4/H2 Ratio
H2/CH4/O2	30-100 Torr	700-1000 °C	400-800 Watts/in^2	2% to 4%

Table 1 List and range of the factors used to map the deposition domain

20 microns Diamond on Strip	CH4/H2 = 2%	883 Watts/meter. °K
50 microns Diamond on Strip	CH4/H2 = 2%	922 Watts/meter. °K
20 microns Diamond on Strip	CH4/H2 = 3.5%	761 Watts/meter. °K
400 microns Free-Standing Diamond	CH4/H2 = 2%	940 Watts/meter. °K

Table 2 Measured thermal conductivity of diamond

Process	Diamond-on-Silicon	Free-Standing Diamond
Condition A	3.39E+08 dyn/cm² tensile	3.65E+06 dyn/cm² tensile
Condition B	2.25E+09 dyn/cm² tensile	1.9E+09 dyn/cm² tensile

Table 3 Measured Stress for SoD and freestanding diamond

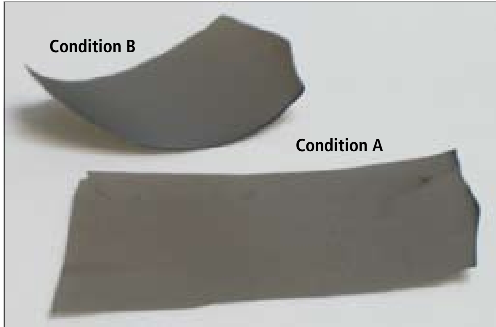


Fig 7 Free-Standing diamond pieces from Table 3

Fig 8 2-inch and 4-inch Free-Standing GaN-on-Diamond wafers

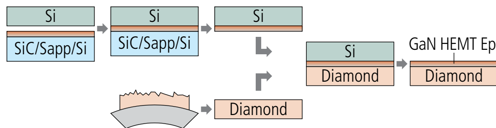


Fig 9a The process for forming a semiconductor-on-diamond composite wafer

Fig 9b A completed 2" wafer

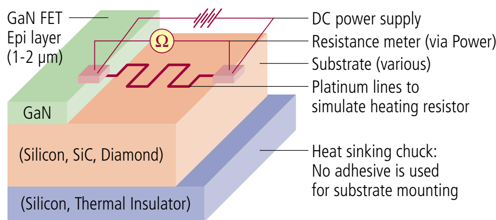
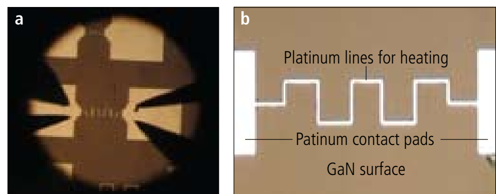


Fig 10 Resistor experiment setup



Figs 11a and 11b Platinum resistor on GaN-on-Diamond

The total stress is the sum of its two components namely the intrinsic stress and the thermal stress:

$$\sigma_T = \sigma_{th} + \sigma_{in}$$

where the σ_T is the total stress, σ_{th} is the thermal stress, σ_{in} is the intrinsic stress.

Knowing the deposition temperature, the thermal stress was easily calculated using the following formula:

$$\sigma_{th} = E_f/(1-\nu) * (\alpha_f - \alpha_s) * (T_{dep} - T_m)$$

where σ_{th} is the thermal stress, E_f and ν are Young's modulus and Poisson ratio respectively for the film, α_f and α_s are the thermal expansion coefficients for the film and substrate respectively, T_{dep} is the deposition temperature, and T_m is the stress measurement temperature.

Using the measured stress data, we optimised our process to fabricate free-standing diamond films with acceptable deflection suitable for integration with GaN. Some of the results of this exercise are presented in Table 3.

Visual example of the change in material flatness is presented in Fig 7. As a result of the stress study, 2-inch and 4-inch diameter diamond-on-silicon substrates were generated and successfully integrated with GaN (Fig 8).

GaN-on-Diamond integration

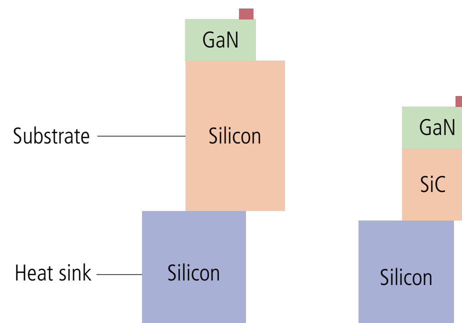
In a proprietary process, GaN FET epi is lifted-off from the host substrate (e.g. Si) and atomically attach it to a polycrystalline CVD diamond substrate. First, the GaN epi is bonded face down to a temporary carrier wafer. Second, the host substrate is etched off using either a wet chemical or dry etch process that is selective to GaN, and the exposed GaN epi backside is specially treated with a nanometer-thin dielectric coating. Finally, the diamond substrate is atomically attached using a proprietary process where the first layer of diamond atoms chemically bonds with the back side of the specially treated GaN epi (Fig 6a and 6b).

Experimental verifications

A simple resistor-based experiment was devised to i) generate FET-like power on a GaN-on-Diamond and other wafer surface, and ii) measure surface temperature changes associated with the power (Fig 10).

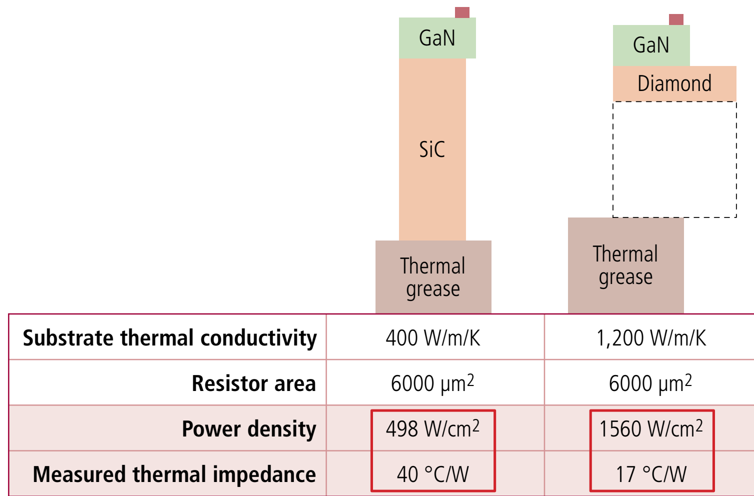
Excellent quality platinum resistor lines were fabricated atop the GaN-on-Diamond as well as GaN-on Silicon and, GaN-on-SiC wafers (Fig 11a and 11b)

An initial side by side evaluation of the results for GaN-on-Silicon and GaN-on-SiC structures revealed that a 3X boost in substrate's thermal conductivity = 3X reduction in substrate's thermal impedance (Fig 12).



Substrate thermal conductivity	150 W/m/K	400 W/m/K
Power density applied to resistor	500 W/cm²	500 W/cm²
Measured thermal impedance	43 °C/W	15 °C/W

Fig 12 Resistor data for GaN on silicon and SiC



Substrate thermal conductivity	400 W/m/K	1,200 W/m/K
Resistor area	6000 μm2	6000 μm2
Power density	498 W/cm2	1560 W/cm2
Measured thermal impedance	40 °C/W	17 °C/W

Fig 13 Resistor data for GaN on Diamond and SiC

Representative GaN-on-Diamond FET data	Vendor-1	Vendor-2
Sheet resistivity (Lehighton)	420 Ω/☐	385 Ω/☐
Drain-Source current I (sat-max)	1000 mA/mm	1200 mA/mm
Contact resistance	0.50 Ω-mm	0.52 Ω-mm

Table 4 Electrical measurement for integrated GaN

A quick comparison of the diamond and SiC structures showed that the use of diamond drops the resistor's thermal impedance by nearly 58% while also allowing a 3X boost in power density (Fig 13).

Subsequent to the resistor study, a preliminary evaluation of FET results revealed that our diamond integration process had no negative effect on GaN epitaxy. The sheet and contact resistance results shown in Table 4, are virtually identical to many published reports of industrial GaN on either Si or SiC [10, 11] indicating a GaN material that is unchanged during the epitaxial transfer process.

Conclusion

A technique for integration of diamond substrate into GaN-on-Diamond was successfully demonstrated. Simple DC data appears to confirm the expected simulation results that, diamond could drive down thermal impedance (°C/W) by as much as 58% compared to SiC. Furthermore, diamond could drive up a GaN FET's power density by 3-fold. ◆

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